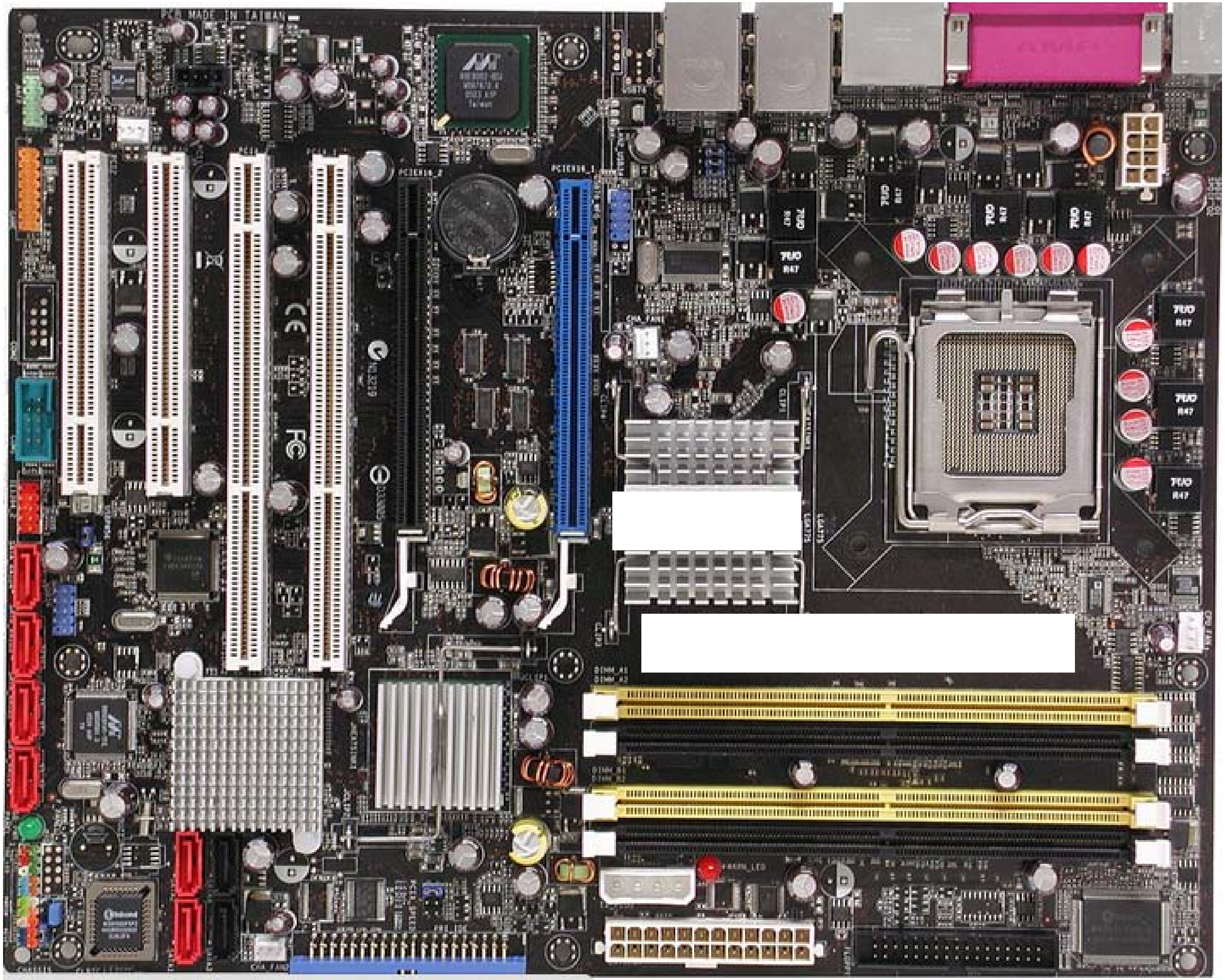
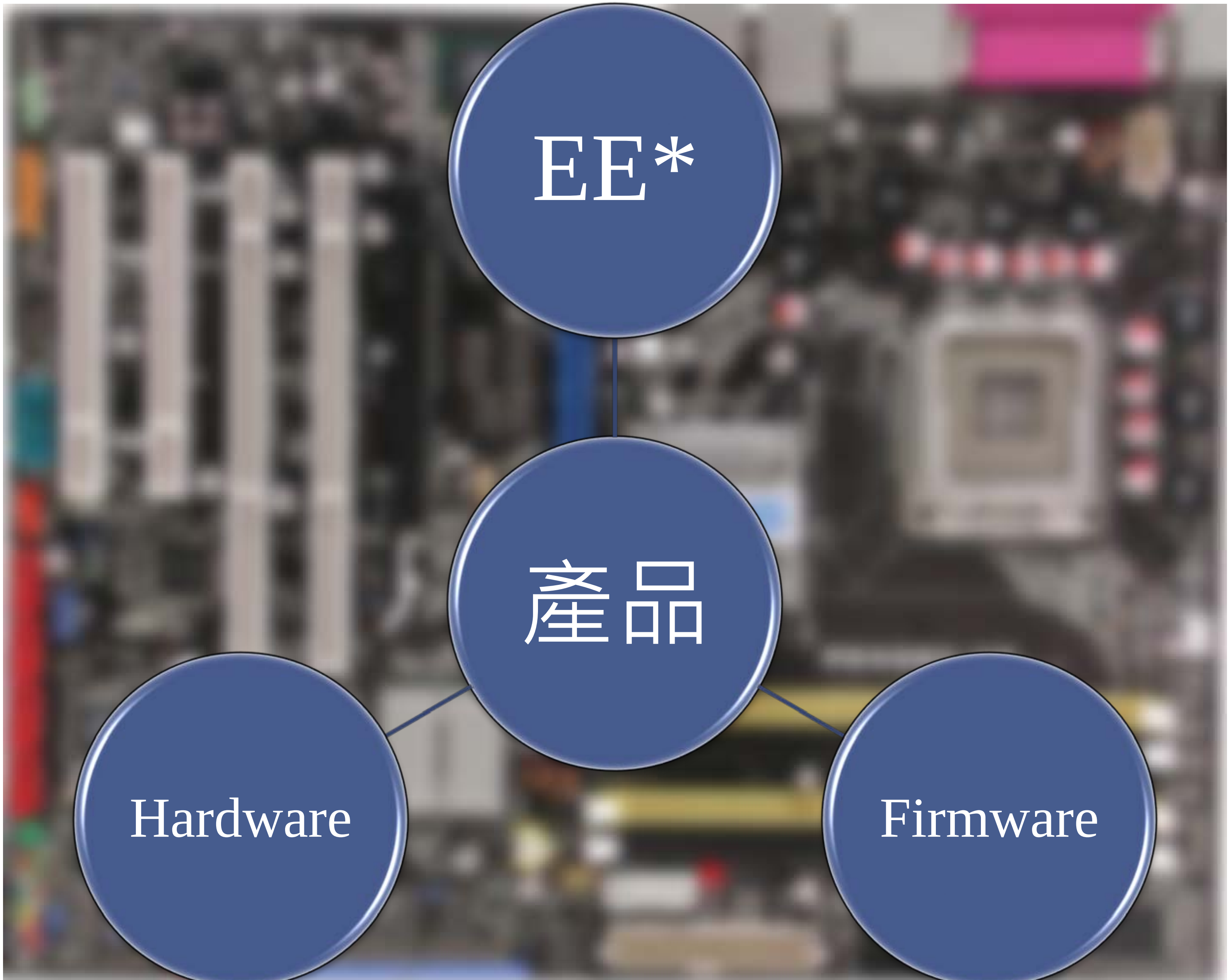
電力電子之回授控制應用

OUTLINE

- 電力電子工程師的角色.
- 如何看懂Datasheet，並評估電源好壞.
- 電力電子之回授控制應用

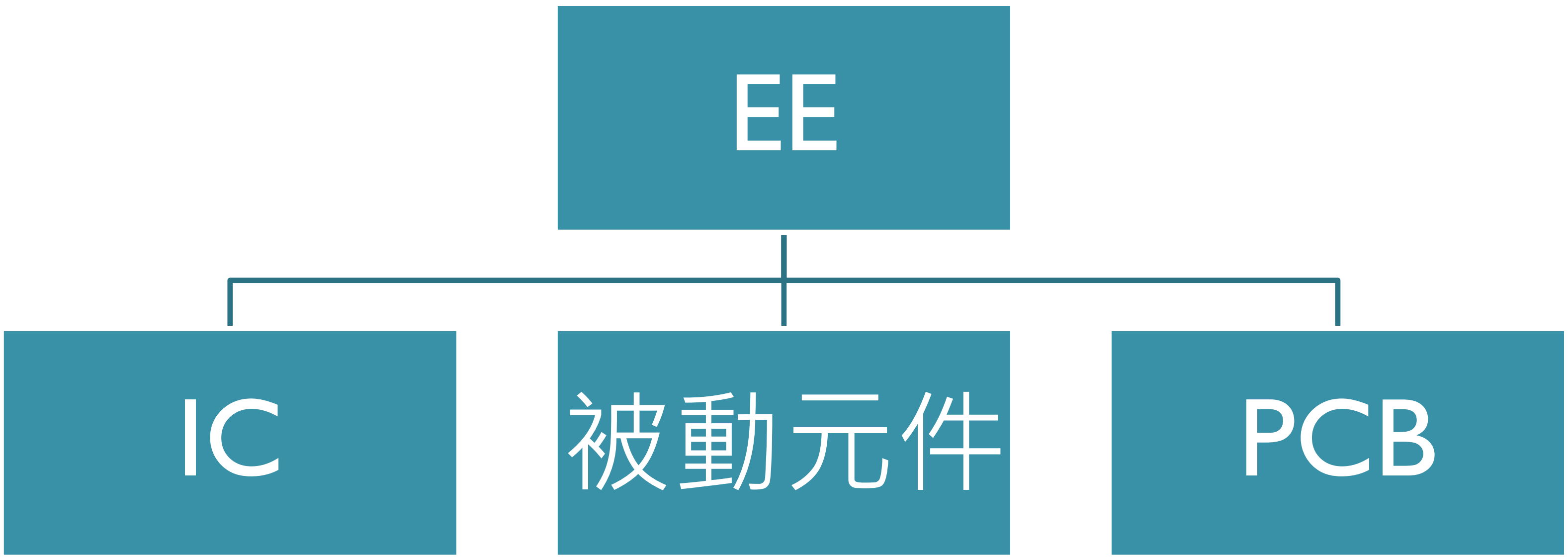



EE*
產品
Hardware
Firmware

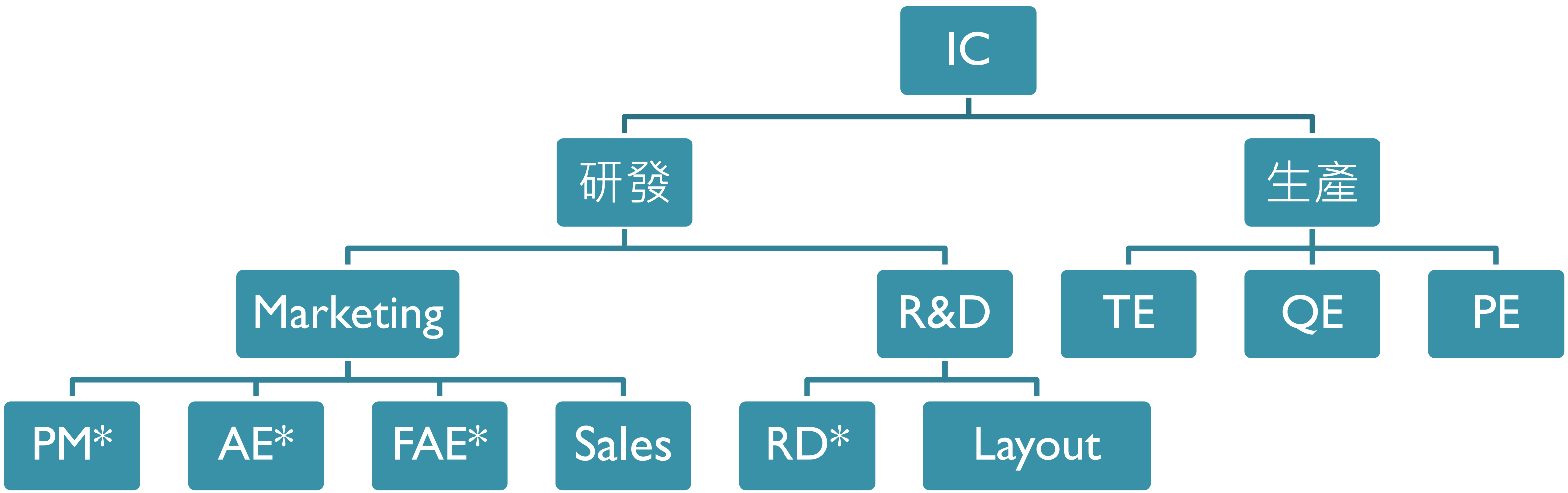
職務內容

- Hardware
  - 應用 數位/類比 IC的能力
- Firmware
  - 軟韌體撰寫
- EE
  - 產品所需之電源規畫與設計

EE需要接洽的事物



IC設計公司的職務



職務工作內容

- PM
  - 產品規畫
- AE
  - 產品規格制定
  - 產品驗證
- FAE
  - 協助客戶處理產品應用問題
- Sales
- RD
  - 產品設計
- Layout
  - IC Layout

職務工作內容

- TE
  - 量產測試(CP : Chip Probing, FT : Final Testing)
- QE
  - 品質工程師
- PE
  - 製程工程師

OUTLINE

- 電力電子工程師的角色.
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TPS6267x

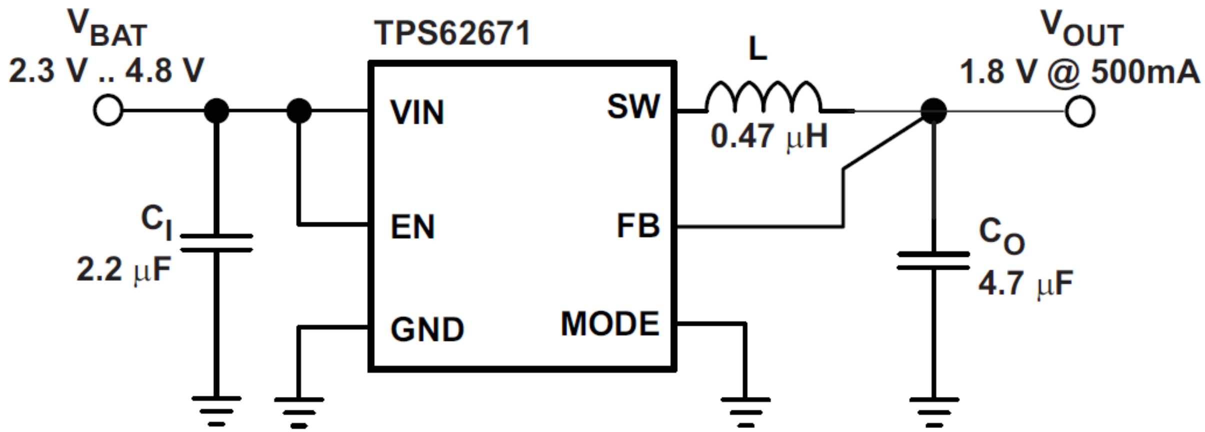
FEATURES

- 92% Efficiency at 6MHz Operation
- 17μA Quiescent Current
- Wide V_{IN} Range From 2.3V to 4.8V
- 6MHz Regulated Frequency Operation
- Spread Spectrum, PWM Frequency Dithering
- *Best in Class* Load and Line Transient
- ±2% Total DC Voltage Accuracy
- Low Ripple Light-Load PFM Mode
- ≥35dB V_{IN} PSRR (1kHz to 10kHz)
- Simple Logic Enable Inputs
- Supports External Clock Presence Detect Enable Input
- Three Surface-Mount External Components Required (One 0603 MLCC Inductor, Two 0402 Ceramic Capacitors)
- Complete Sub 0.33-mm Component Profile Solution
- Total Solution Size <10 mm^2
- Available in a 6-Pin NanoFree™ (CSP) Ultra-Thin Packaging, 0,4mm Max. Height

APPLICATIONS

- Cell Phones, Smart-Phones
- Camera Module Embedded Power
- Digital TV, WLAN, GPS and Bluetooth™ Applications
- DC/DC Micro Modules

Smallest Solution Size Application



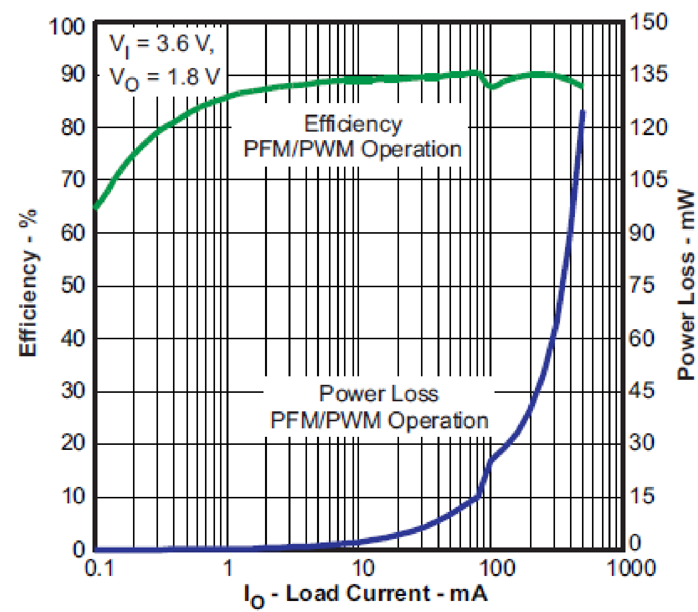
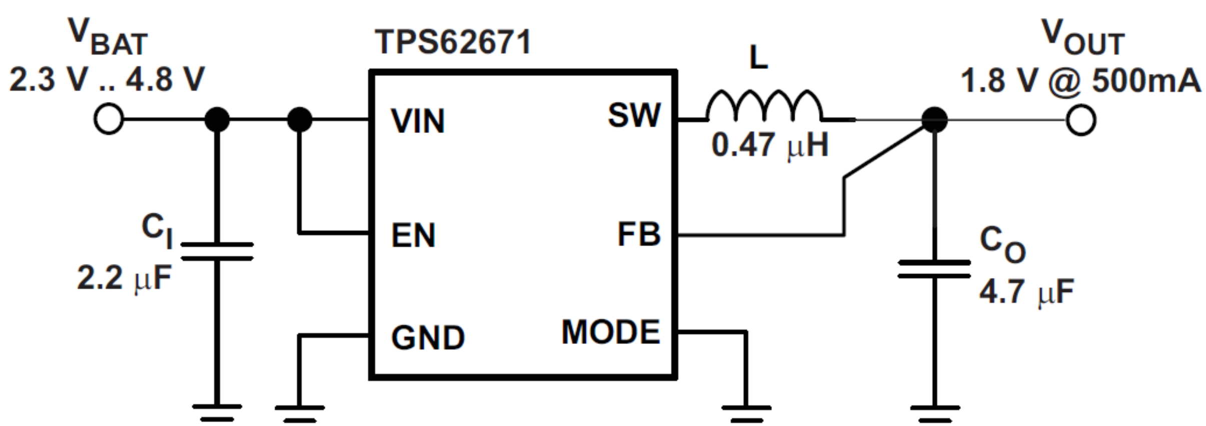


Figure 1. Efficiency vs. Load Current

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
FB	C1	I	Output feedback sense input. Connect FB to the converter's output.
VIN	A2	I	Power supply input.
SW	B1	I/O	This is the switch pin of the converter and is connected to the drain of the internal Power MOSFETs.
EN	B2	I	This is the enable pin of the device. Connecting this pin to ground forces the device into shutdown mode. Pulling this pin to V_I enables the device. If an external clock (4MHz to 27MHz) is detected the device will automatically power up. This pin must not be left floating and must be terminated.
MODE	A1	I	This is the mode selection pin of the device. This pin must not be left floating and must be terminated.
			MODE = LOW: The device is operating in regulated frequency pulse width modulation mode (PWM) at high-load currents and in pulse frequency modulation mode (PFM) at light load currents. MODE = HIGH: Low-noise mode enabled, regulated frequency PWM operation forced.
GND	C2	–	Ground pin.



Electrical Characteristics

ELECTRICAL CHARACTERISTICS

Minimum and maximum values are at V_I = 2.3V to 5.5V, V_O = 1.8V, EN = 1.8V, AUTO mode and T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_I = 3.6V, V_O = 1.8V, EN = 1.8V, AUTO mode and T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_Q	Operating quiescent current	TPS62671 TPS62672 TPS62675 TPS62679	I_O = 0mA. Device not switching		17	40	µA
		TPS62671	I_O = 0mA, PWM mode		5.5		mA
		TPS62674 TPS62679	I_O = 0mA, PWM mode		5.0		mA
$I_{(SD)}$	Shutdown current		EN = GND		0.2	1	µA
UVLO	Undervoltage lockout threshold				2.05	2.1	V
ENABLE, MODE							
V_{IH}	High-level input voltage	TPS62671 TPS62672 TPS62675		1.0			V
V_{IL}	Low-level input voltage					0.4	V
I_{lkg}	Input leakage current		Input connected to GND or VIN		0.01	1.5	µA
V_{IH}	High-level input voltage (ENABLE)	TPS62674 TPS62679		1.26			V
	High-level input voltage (MODE)			1.0			V
V_{IL}	Low-level input voltage (ENABLE)					0.54	V
	Low-level input voltage (MODE)	TPS62679				0.4	V
I_{lkg}	Input leakage current	TPS62674 TPS62679	Input connected to GND or VIN		0.01	1.5	µA
C_{IN}	Input capacitance (ENABLE)				5		pF

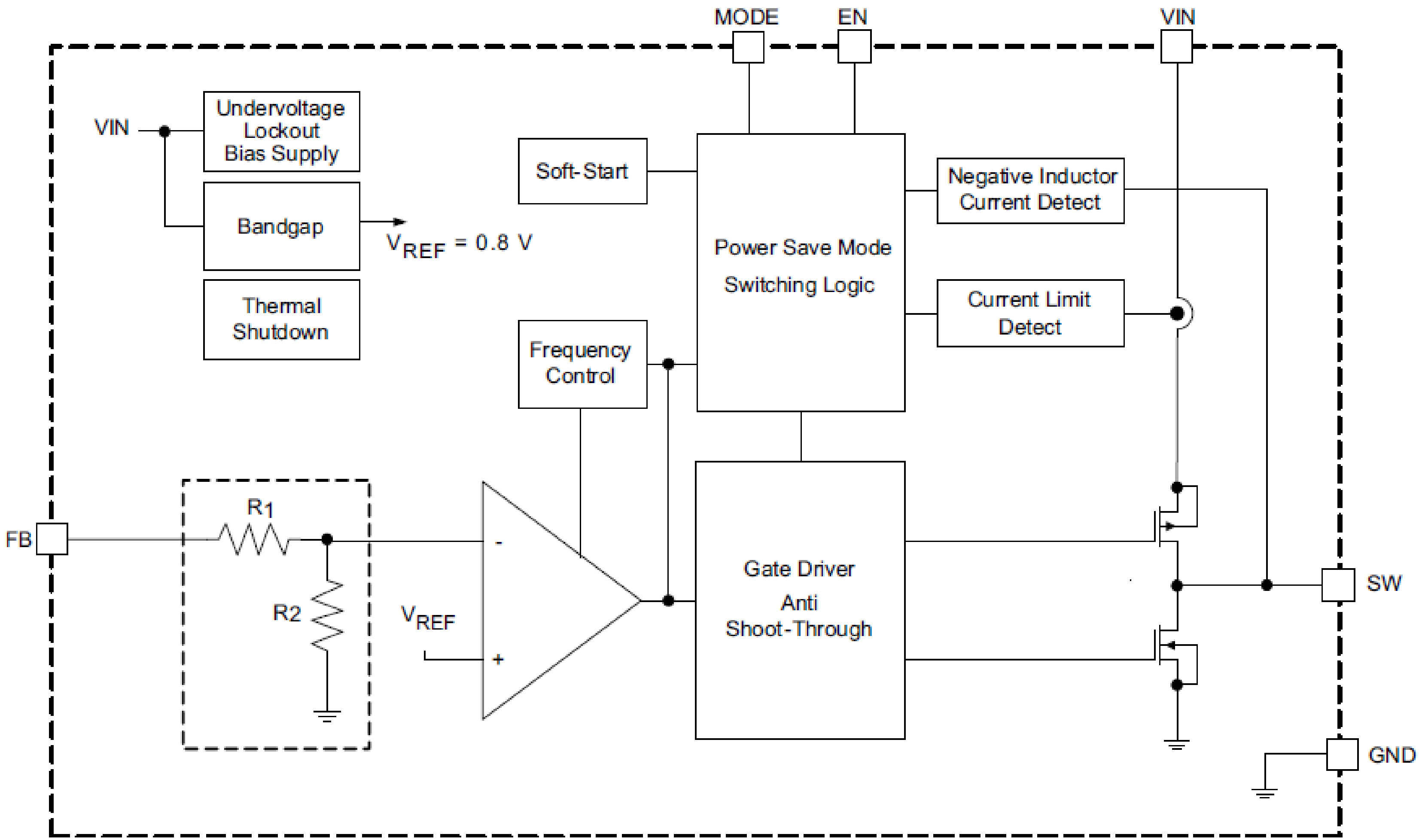
Electrical Characteristics

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
EXTCLK	Clock presence detect frequency	TPS62674 TPS62679			4		27	MHz
	Clock presence detect duty cycle				40		60	%
POWER SWITCH								
$r_{DS(on)}$	P-channel MOSFET on resistance		$V_I = V_{(GS)} = 3.6V$. PWM mode			170		mΩ
			$V_I = V_{(GS)} = 2.5V$. PWM mode			230		mΩ
I_{lkg}	P-channel leakage current, PMOS		$V_{(DS)} = 5.5V$, $-40°C \le T_J \le 85°C$				1	μA
$r_{DS(on)}$	N-channel MOSFET on resistance		$V_I = V_{(GS)} = 3.6V$. PWM mode			120		mΩ
			$V_I = V_{(GS)} = 2.5V$. PWM mode			180		mΩ
I_{lkg}	N-channel leakage current, NMOS		$V_{(DS)} = 5.5V$, $-40°C \le T_J \le 85°C$				2	μA
r_{DIS}	Discharge resistor for power-down sequence					70	150	Ω
	P-MOS current limit		$2.3V \le V_I \le 4.8V$. Open loop	TPS62671 TPS62672 TPS62674 TPS62679	900	1000	1150	mA
			$2.3V \le V_I \le 4.8V$. Open loop	TPS62675	1000	1100	1250	mA
	Input current limit under short-circuit conditions		V_O shorted to ground			12		mA
	Thermal shutdown					140		°C
	Thermal shutdown hysteresis					10		°C
OSCILLATOR								
f_{SW}	Oscillator center frequency	TPS62671 TPS62672 TPS62675	$I_O = 0mA$. PWM operation		5.4	6	6.6	MHz
	Oscillator center frequency	TPS62674 TPS62679	$I_O = 0mA$. PWM operation		4.9	5.45	6.0	MHz

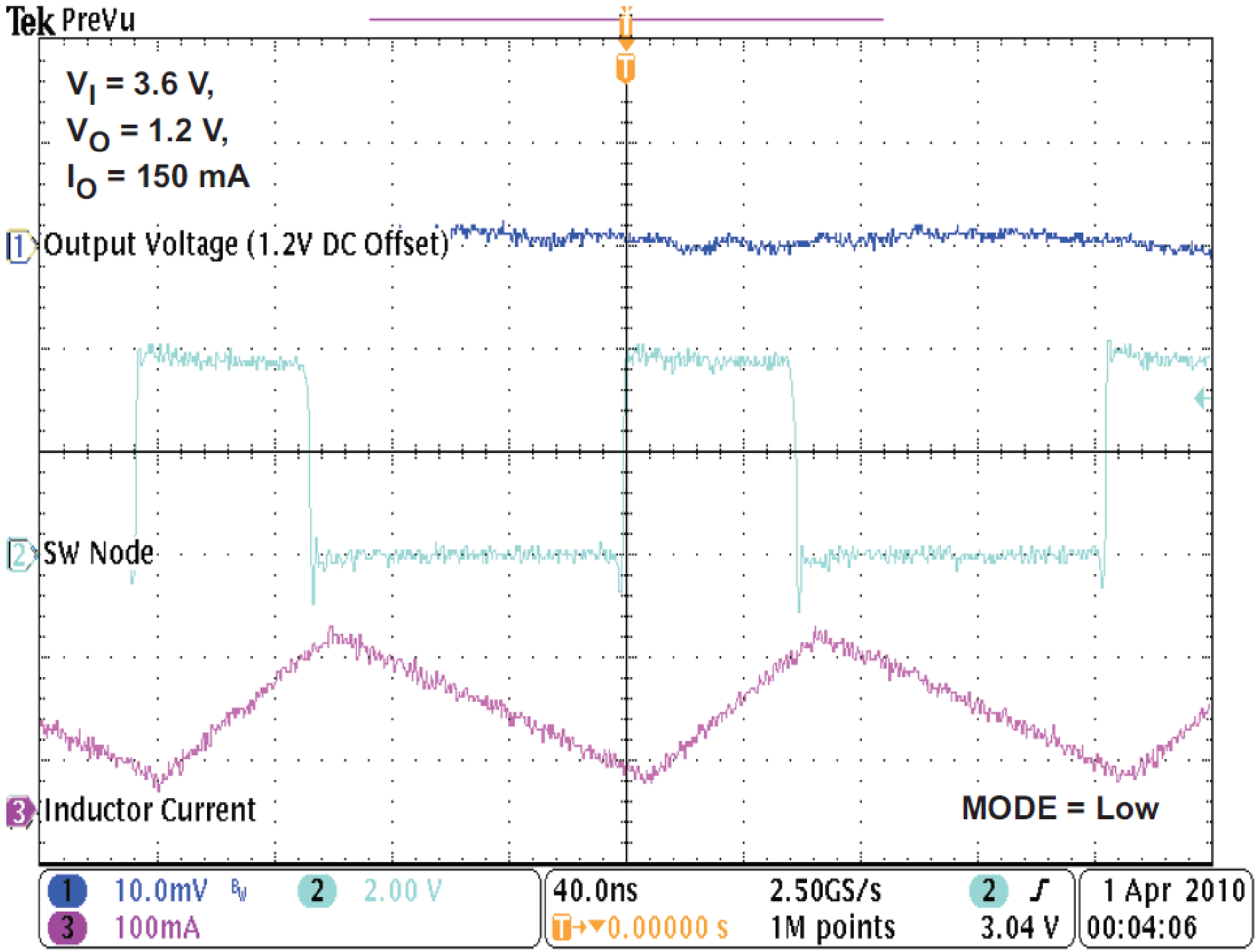
Electrical Characteristics

OUTPUT							
V_{OUT}	Regulated DC output voltage	TPS62671 TPS62672 TPS62679	$2.3V \le V_I \le 4.8V$, $0mA \le I_O \le 500$ mA PFM/PWM operation	$0.98 \times V_{NOM}$	V_{NOM}	$1.03 \times V_{NOM}$	V
			$2.3V \le V_I \le 5.5V$, $0mA \le I_O \le 500$ mA PFM/PWM operation	$0.98 \times V_{NOM}$	V_{NOM}	$1.04 \times V_{NOM}$	V
			$2.3V \le V_I \le 5.5V$, $0mA \le I_O \le 500$ mA PWM operation	$0.98 \times V_{NOM}$	V_{NOM}	$1.02 \times V_{NOM}$	V
		TPS62674	$2.3V \le V_I \le 5.5V$, $0mA \le I_O \le 500$ mA PWM operation	$0.98 \times V_{NOM}$	V_{NOM}	$1.02 \times V_{NOM}$	V
		TPS62675	$2.3V \le V_I \le 4.8V$, $0mA \le I_O \le 650$ mA PFM/PWM operation	$0.98 \times V_{NOM}$	V_{NOM}	$1.03 \times V_{NOM}$	V
			$2.3V \le V_I \le 5.5V$, $0mA \le I_O \le 650$ mA PWM operation	$0.98 \times V_{NOM}$	V_{NOM}	$1.02 \times V_{NOM}$	V
	Line regulation		$V_I = V_O + 0.5V$ (min 2.3V) to 5.5V, $I_O = 200$ mA		0.23		%/V
	Load regulation		$I_O = 0mA$ to 500 mA. PWM operation		–0.00045		%/mA
	Feedback input resistance				480		kΩ
ΔV_O	Power-save mode ripple voltage	TPS62671	$I_O = 1mA$, $V_O = 1.8$ V		14		mV_{PP}
		TPS62675 TPS62679	$I_O = 1mA$, $V_O = 1.2$ V		16		mV_{PP}
	Start-up time	TPS62671	$I_O = 0mA$, Time from active EN to V_O		130		µs
		TPS62674	$I_O = 0mA$, Time from EXTCLK clock active to V_O		125		µs
		TPS62679	$I_O = 0mA$, Time from EXTCLK clock active to V_O L = 1µH DCR = 240mΩ 0603 (TY CKP1608S1R0) C_O = 2.2µF 4V 0402 (TY AMK105BJ225MP)		430		µs

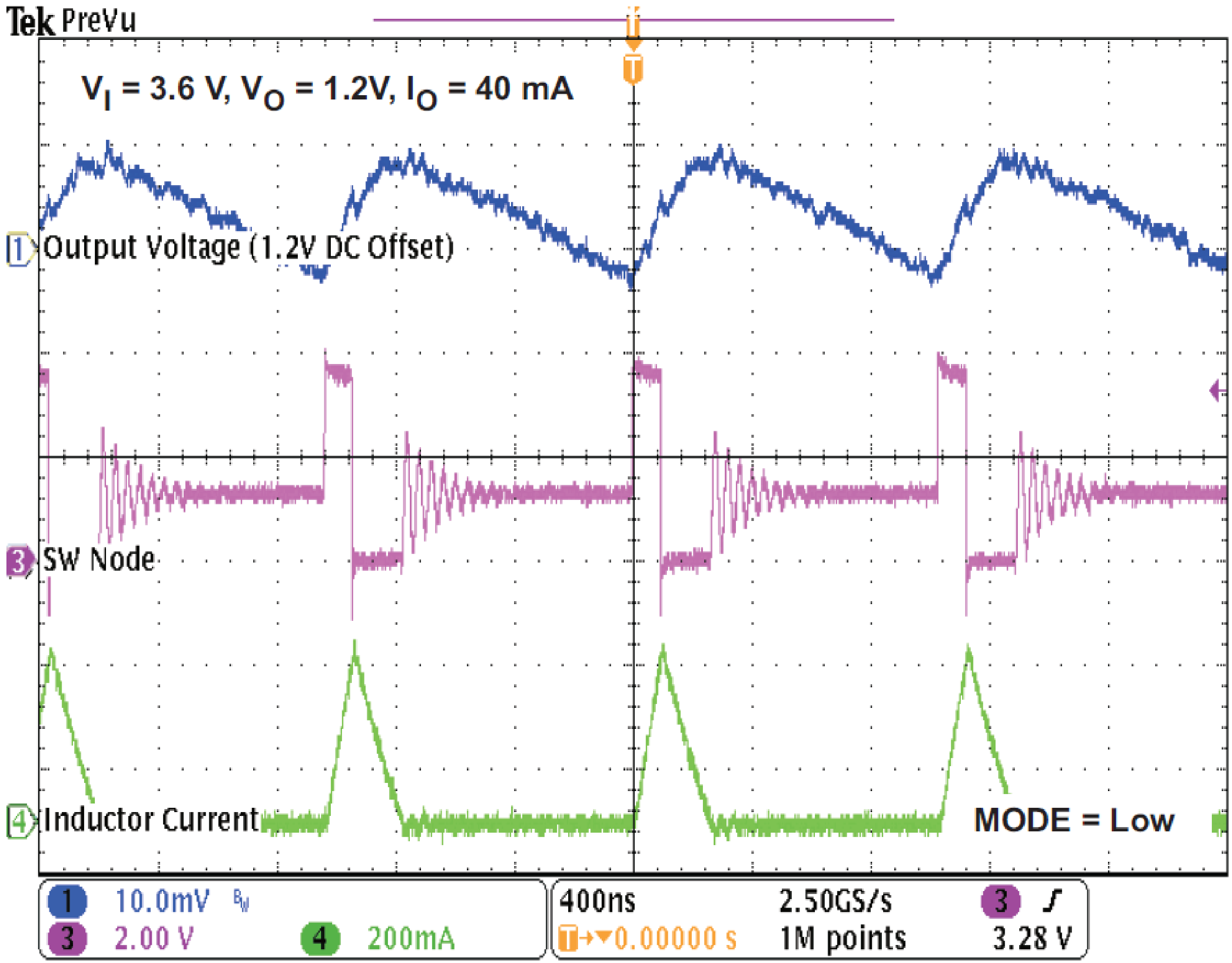
FUNCTIONAL BLOCK DIAGRAM



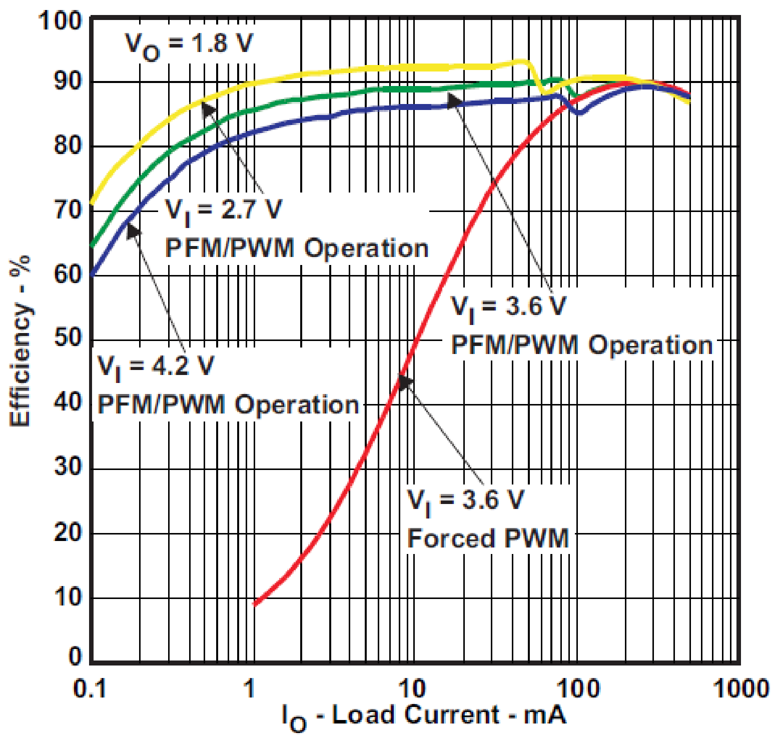
PWM Operation

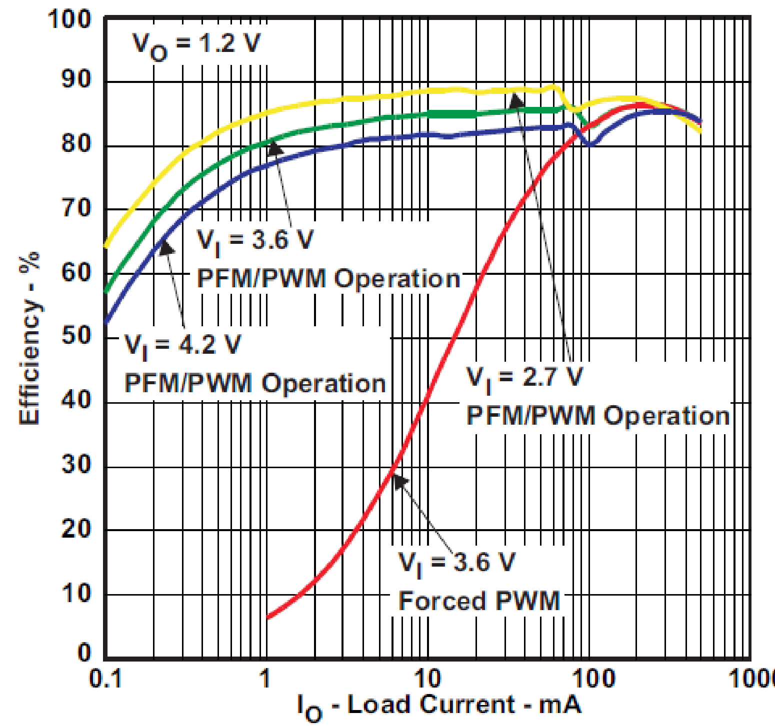


Power Save Mode Operation

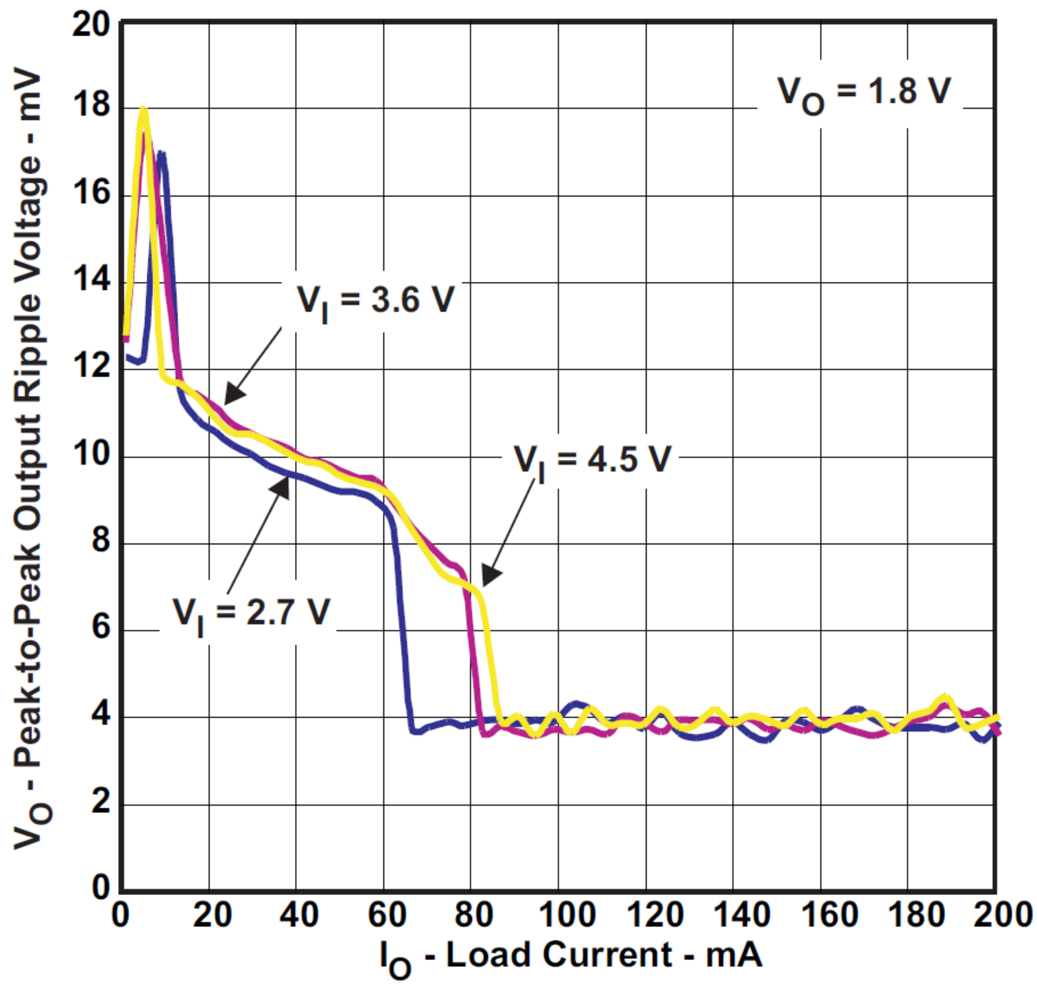


Efficiency vs Load Current

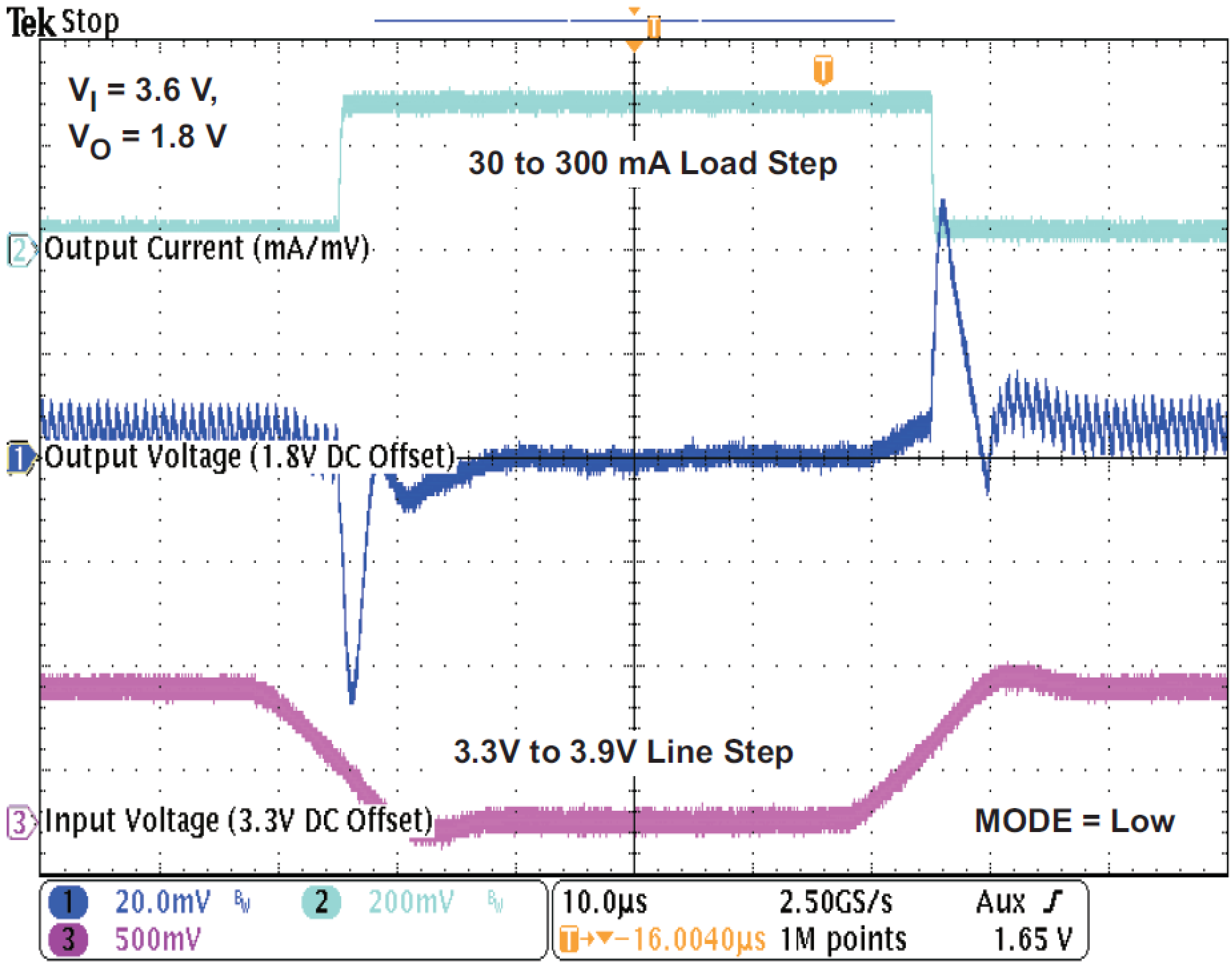




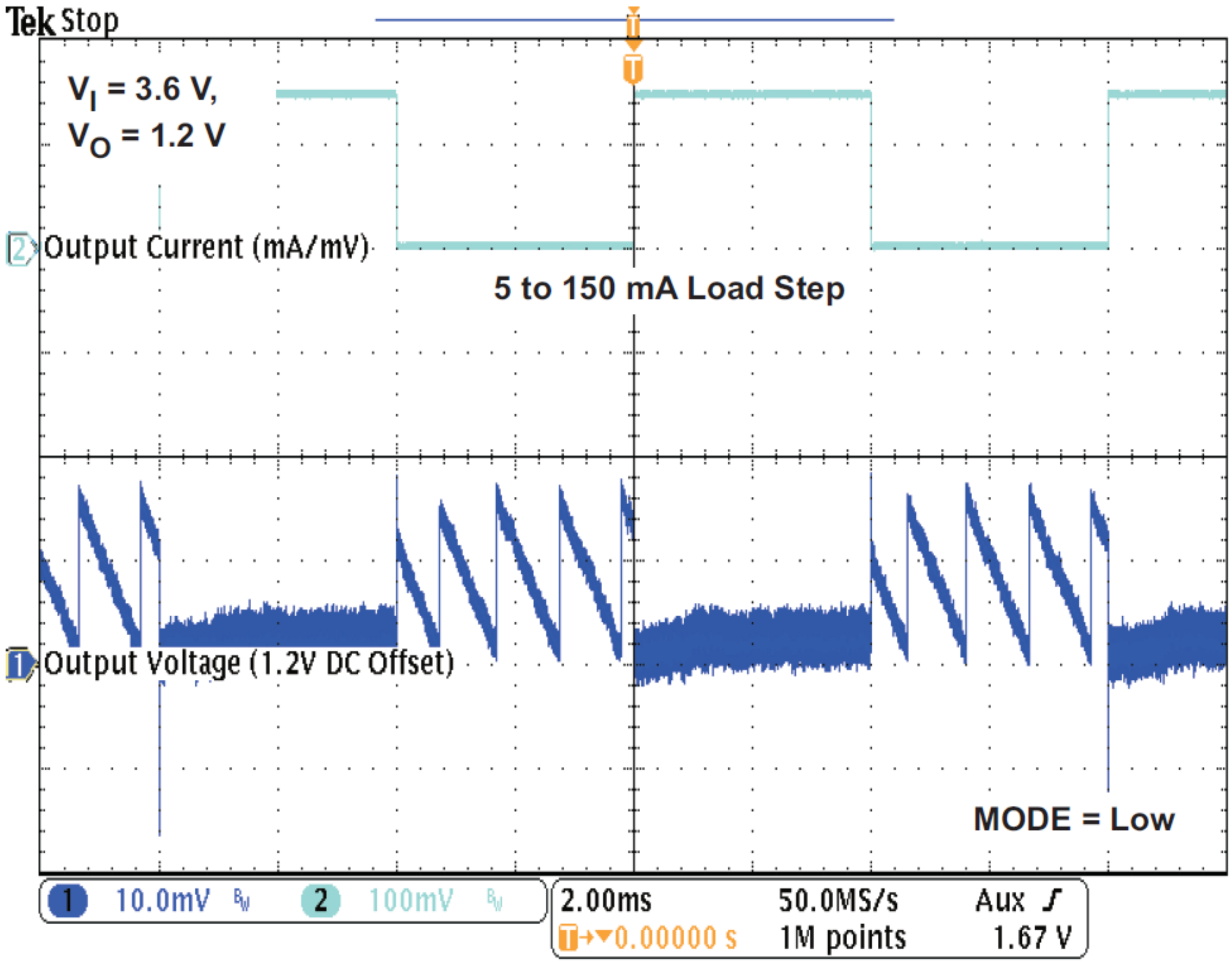
Peak to Peak Output Ripple Voltage vs Load Current



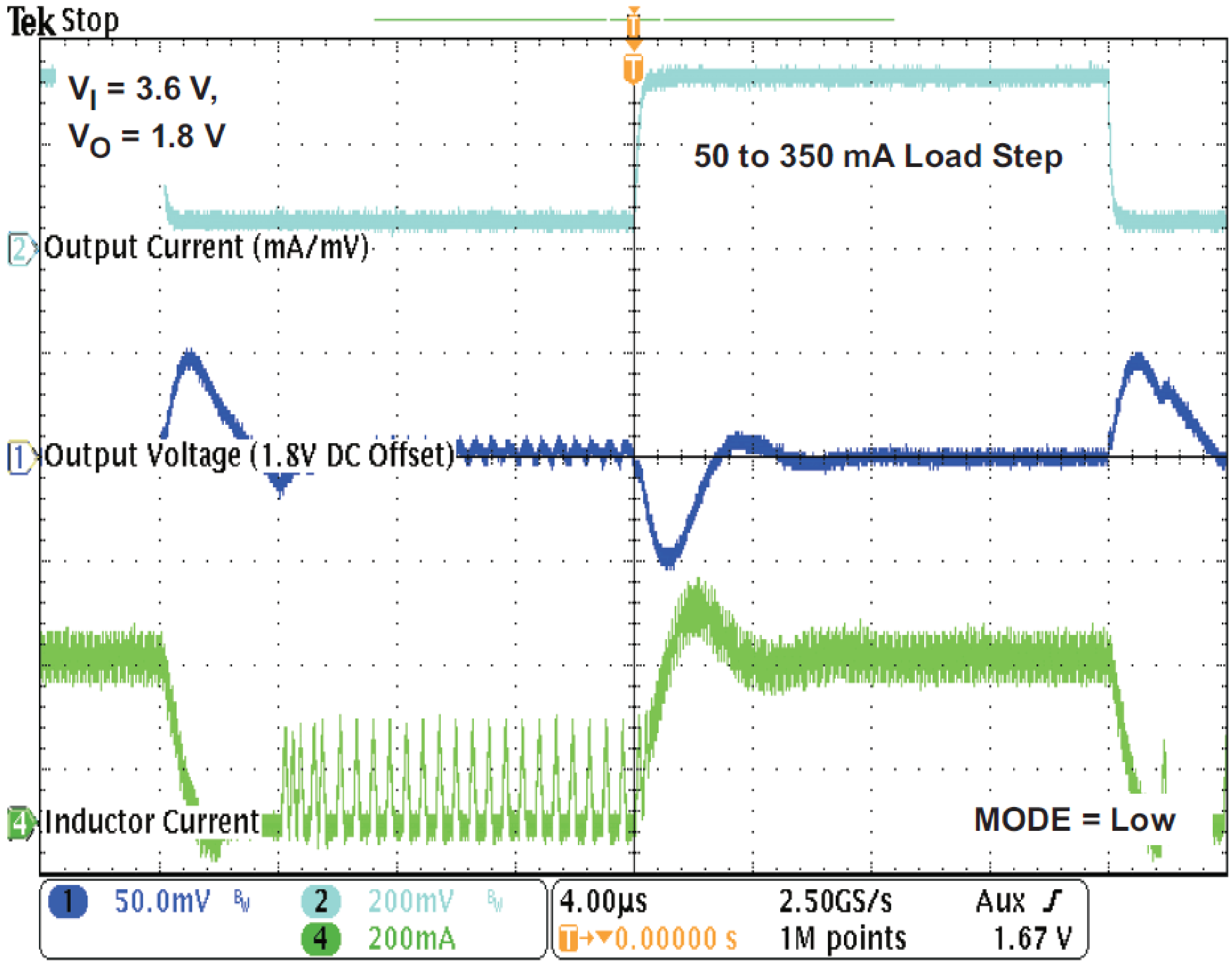
Combined Line/Load Transient Response



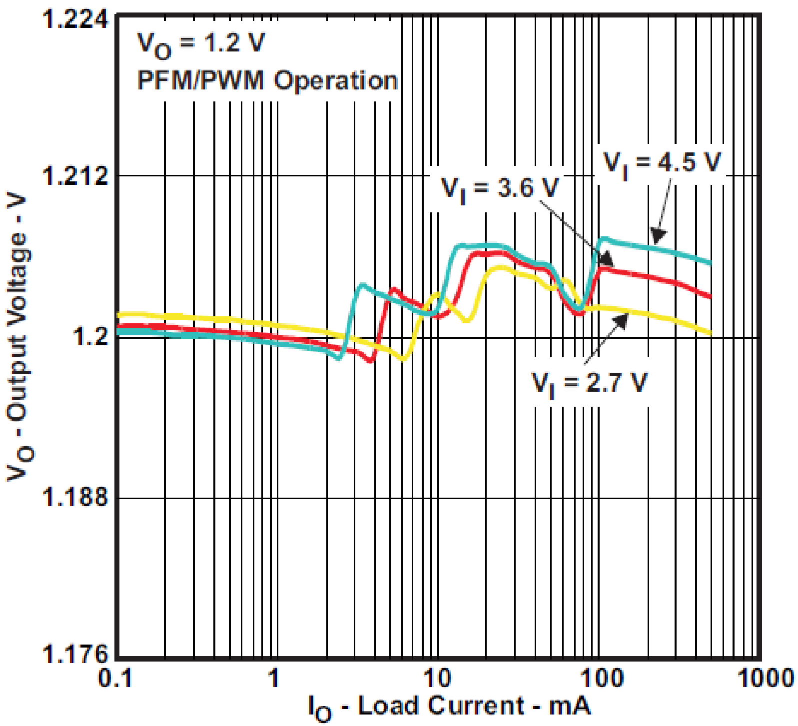
Load Transient Response in PFM/PWM Operation

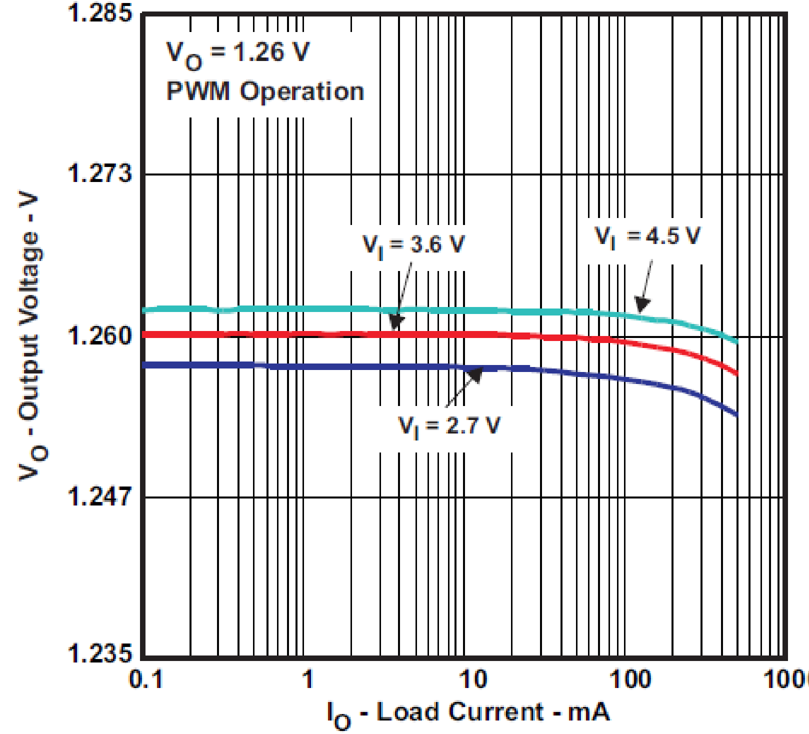


Load Transient response in PFM/PWM Operation

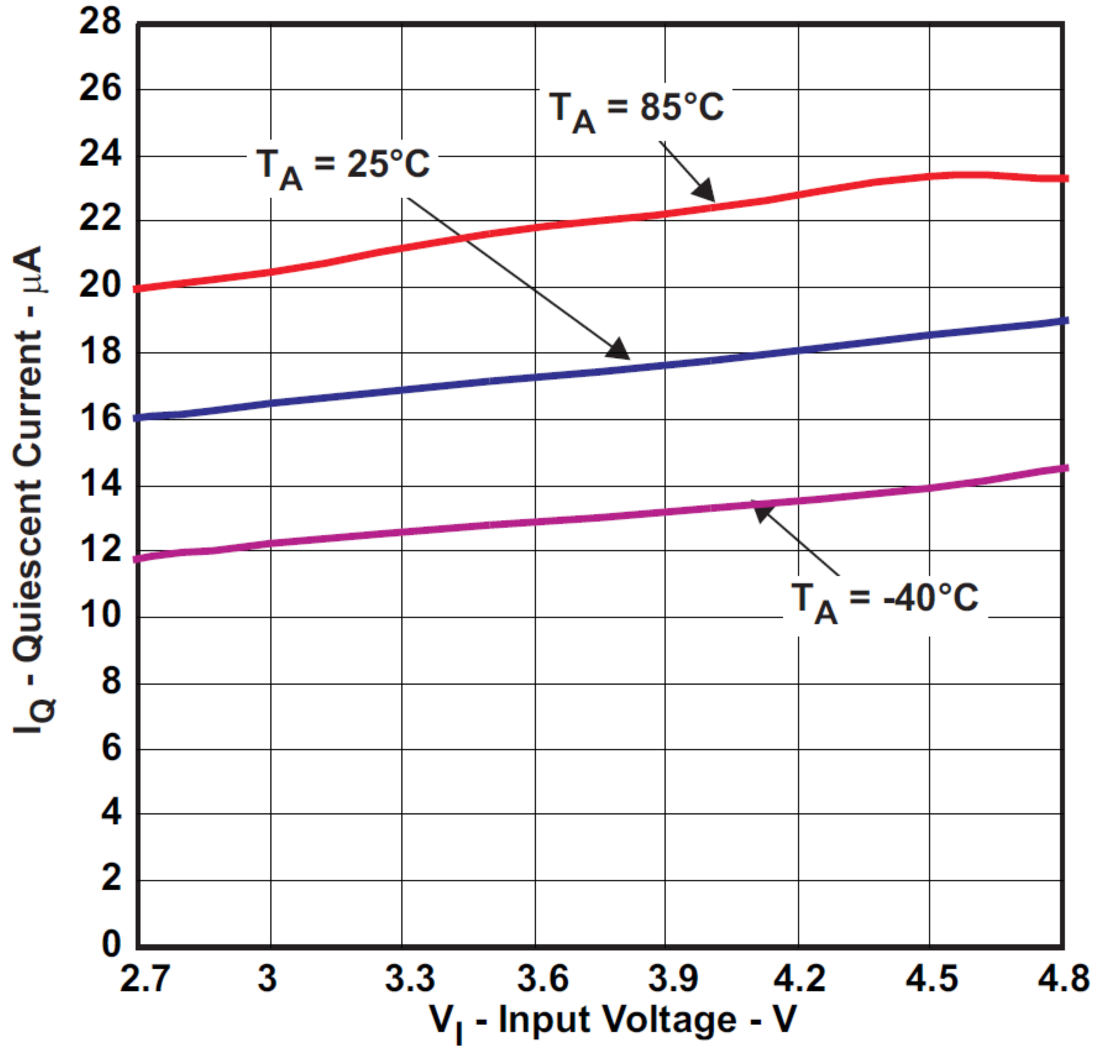


DC Output Voltage vs Load Current

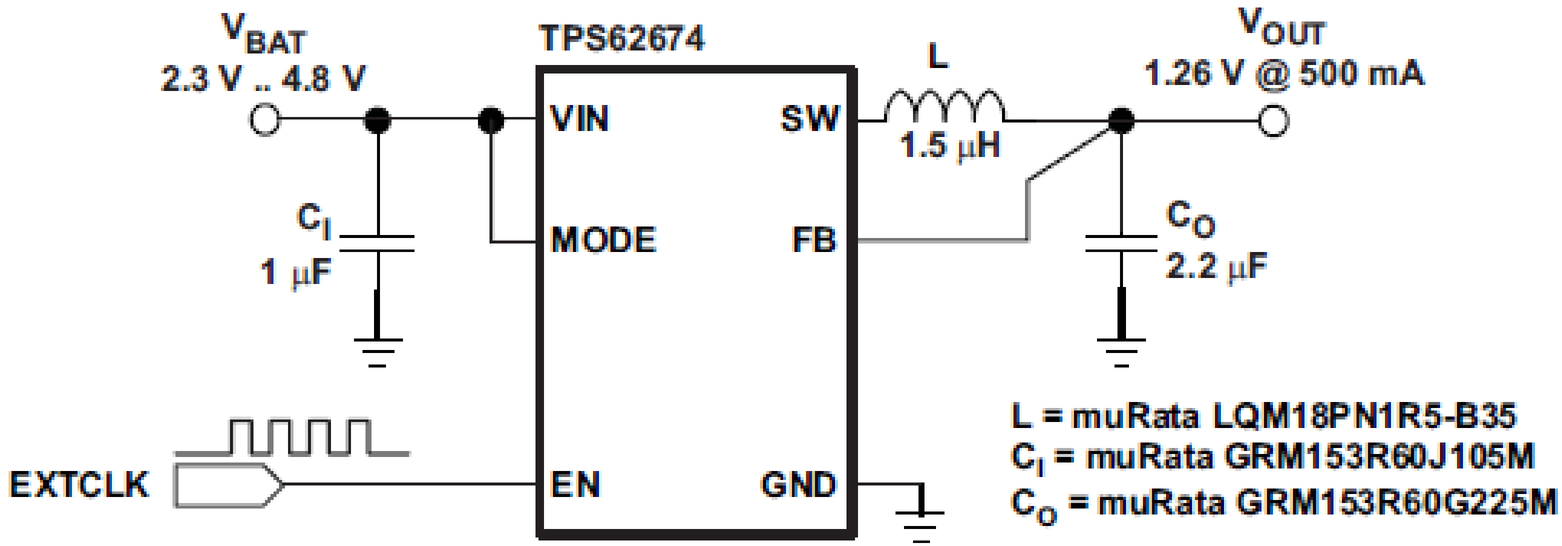




Quiescent Current vs Input Voltage

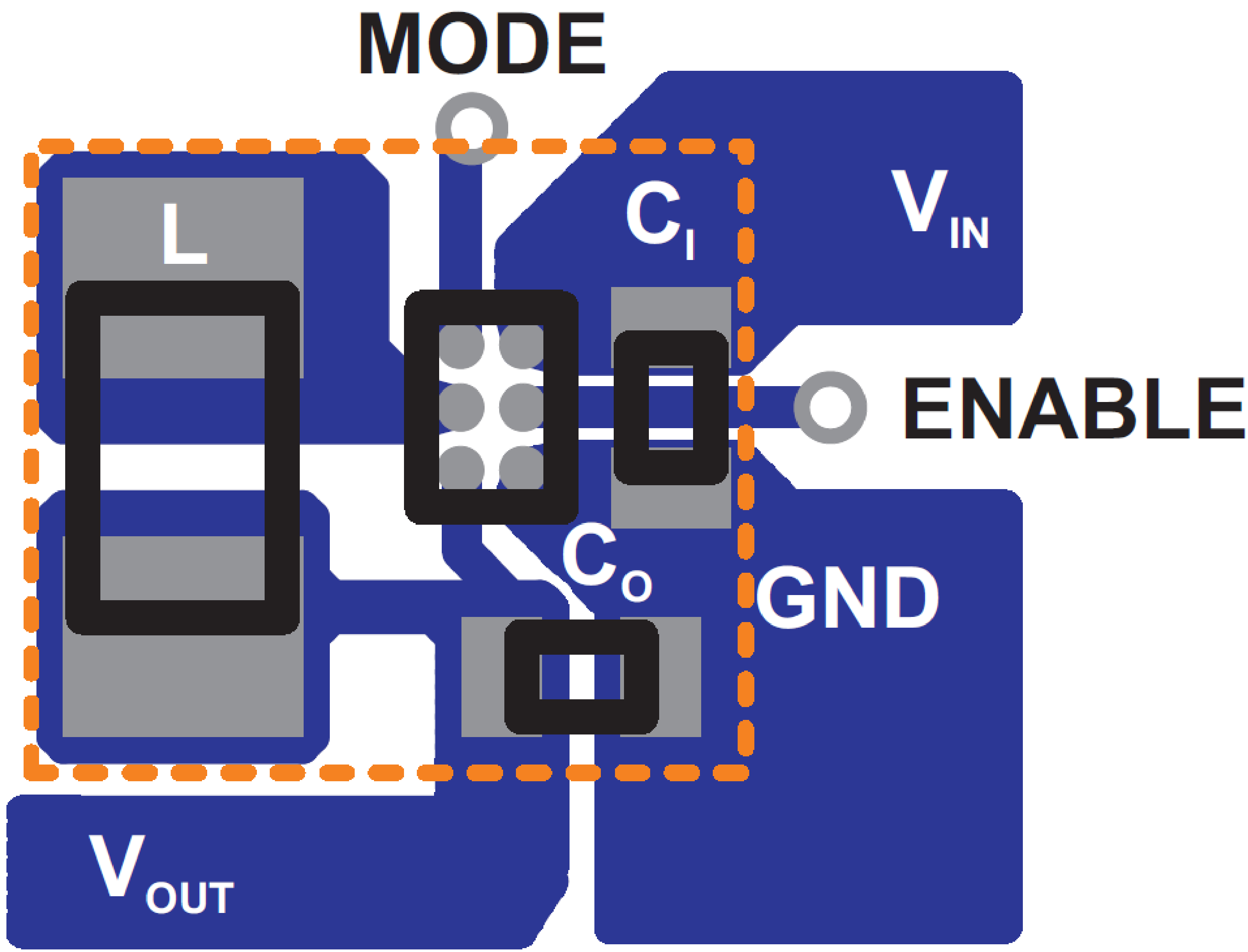


Layout



VBAT
2.3 V .. 4.8 V
TPS62674
L
VOUT
1.26 V @ 500 mA
VIN
SW
1.5 μH
CI
1 μF
MODE
FB
CO
2.2 μF
L = muRata LQM18PN1R5-B35
CI = muRata GRM153R60J105M
CO = muRata GRM153R60G225M
EXTCLK
EN
GND

Layout



OUTLINE

- 電力電子工程師的角色.
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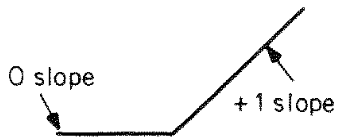
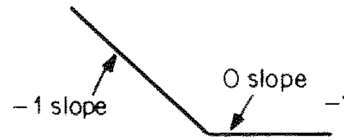
Fundamental of Bode Plot

One zero



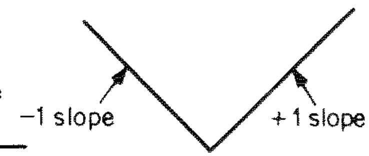
(a)

One Zero



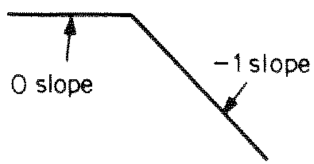
(b)

Two zeros



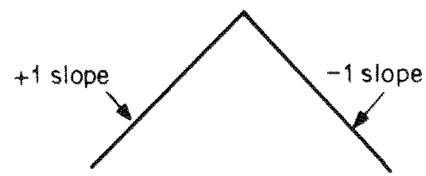
(c)

One Pole



(d)

Two Poles



(e)

One zero : the phase will lead 90^o finally ($+90^o$)

One pole : the phase will lag 90^o finally (-90^o)

-1 slope = -20dB/decade +1 slope = +20dB/decade

※ **db=20* log Vo/Vi**

Fundamental of Bode Plot

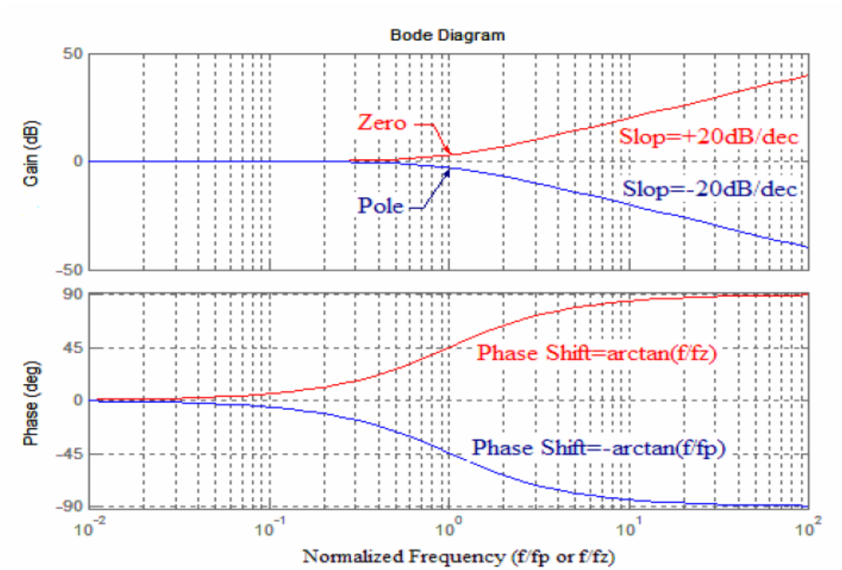
Pole and Zero :

Transfer function use Laplace as below:

$$G(s) = \frac{K(s+z_1)\cdots(s+z_m)}{(s+p_1)(s+p_2)\cdots(s+p_n)}$$

$s = -z_1, -z_2, \cdot \cdot \cdot, -z_m$ -Z_m is Zero(S- Z_m =0).

$s = -p_1, -p_2, \cdot \cdot \cdot, -p_n$ -P_m is Pole(S+ P_m =0.

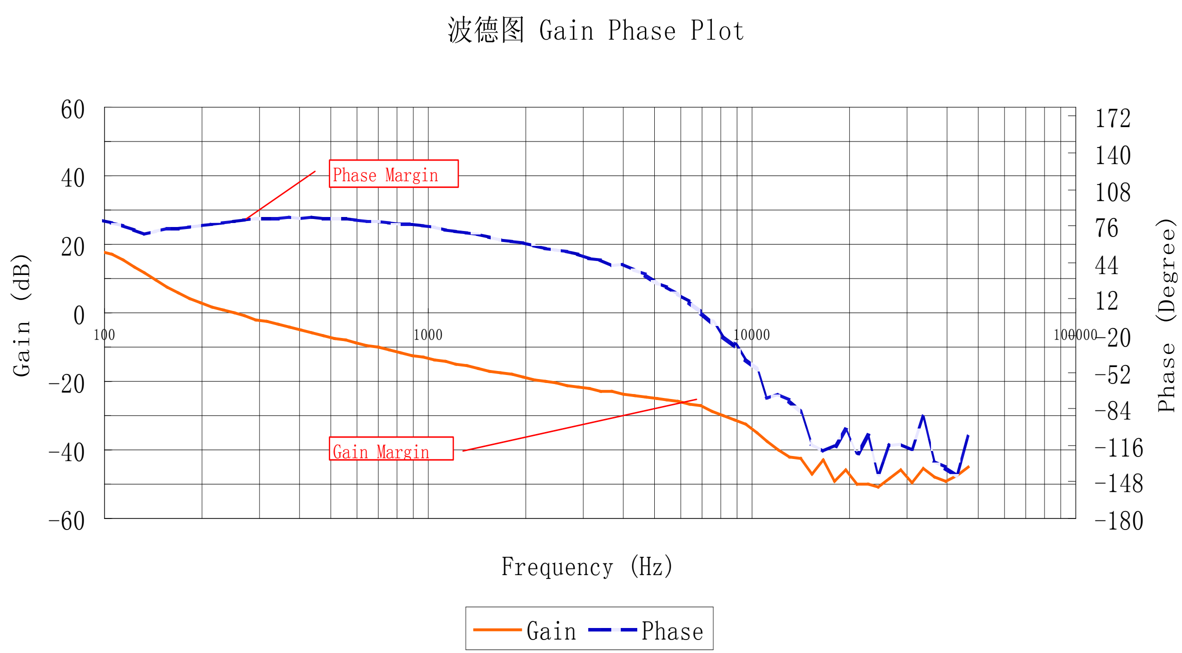


Stable loop gain should satisfy

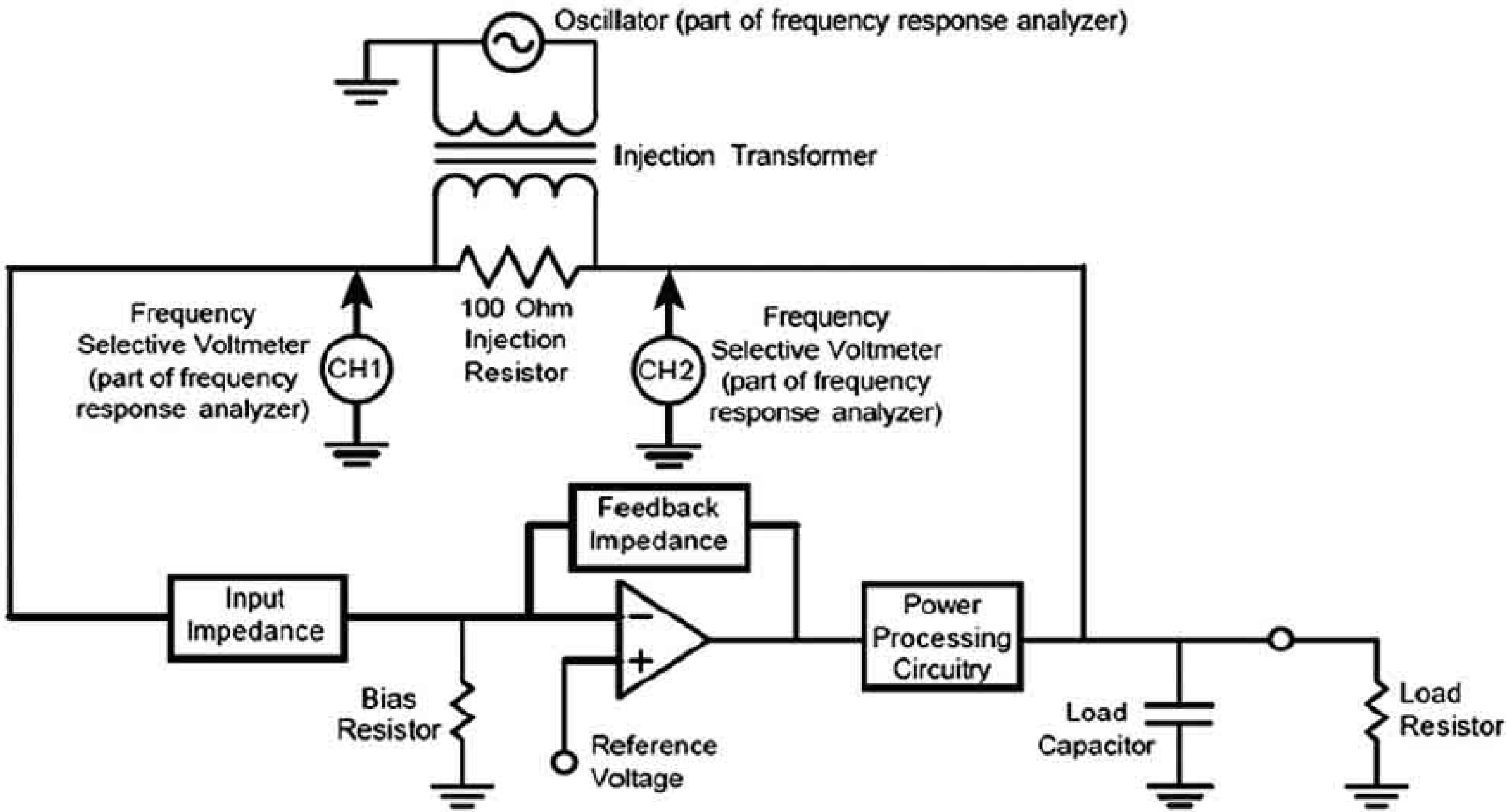
I. Provide the desired Bandwidth between (1/5~1/10)*Fsw.

II. The gain slope as it pass through the crossover frequency should be –1(-20dB/decade).

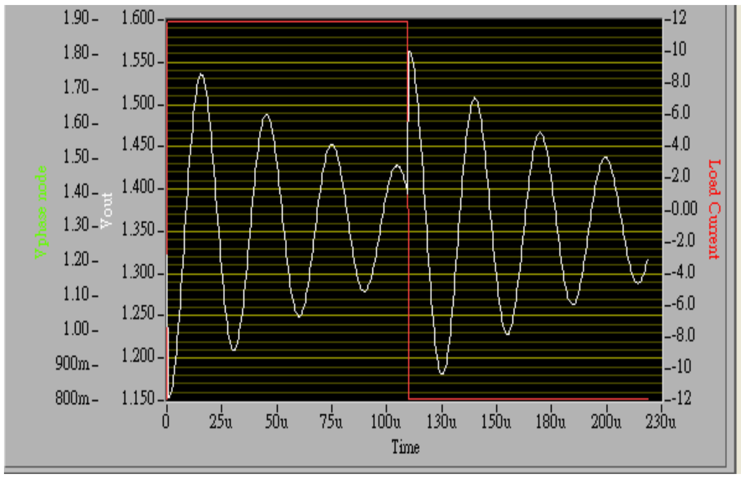
III. Provide the desired phase margin 45º~60º.



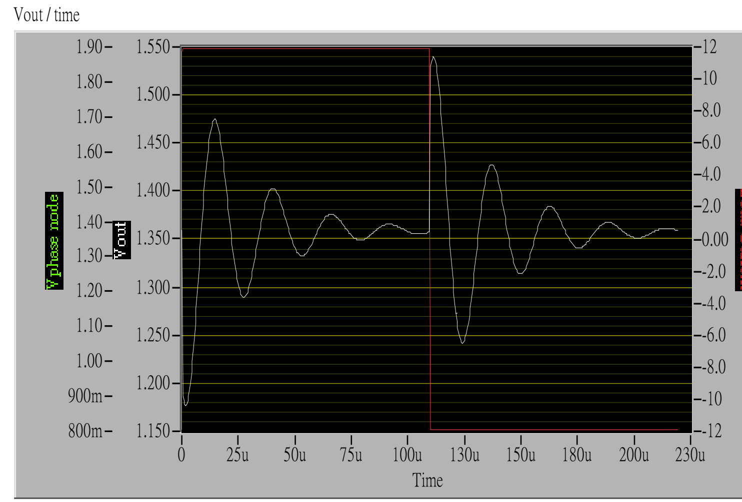
Measurement Bode Plot



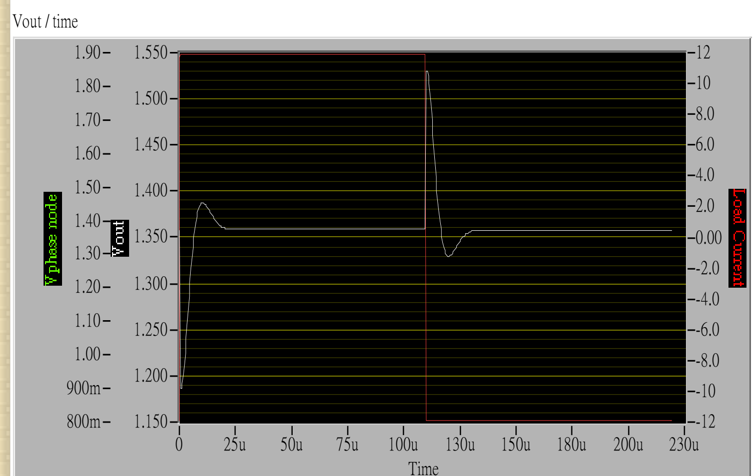
Transient Response



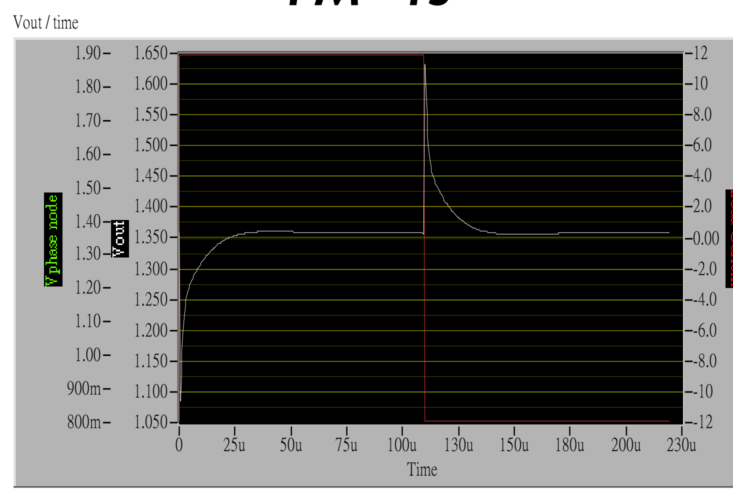
PM =5 °



PM =15 °



PM =45 °

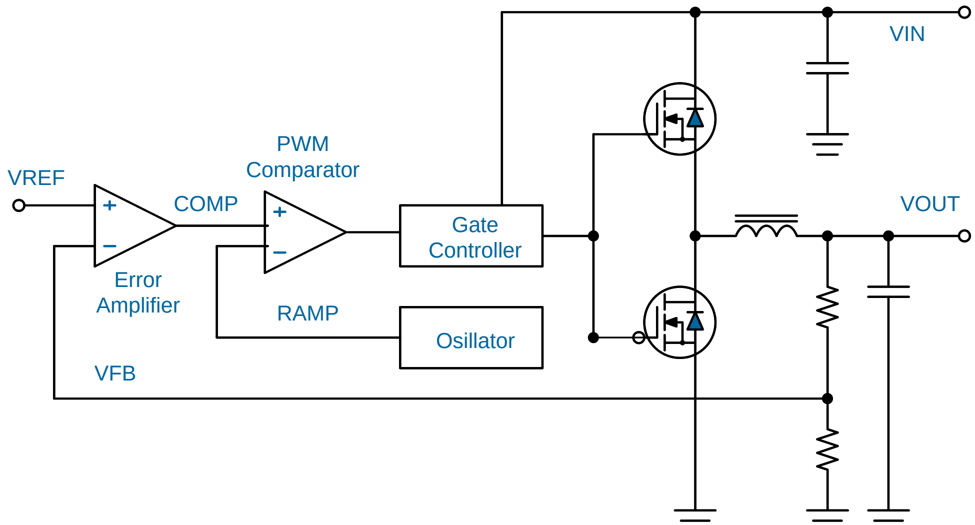


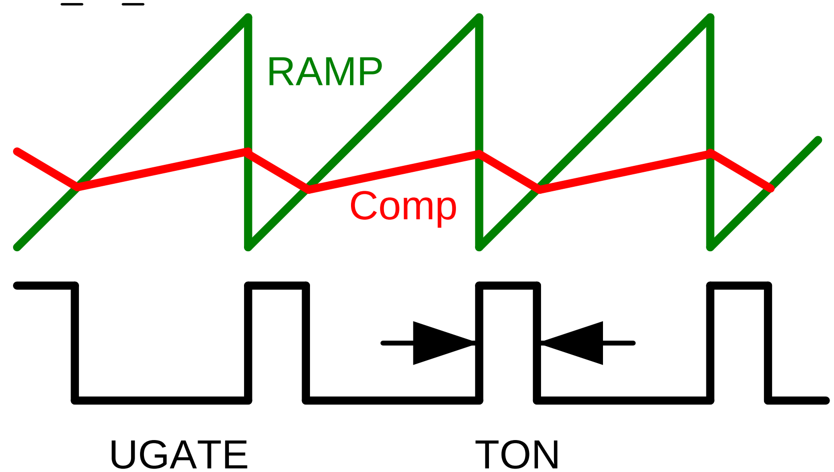
PM =100 °

補償方法

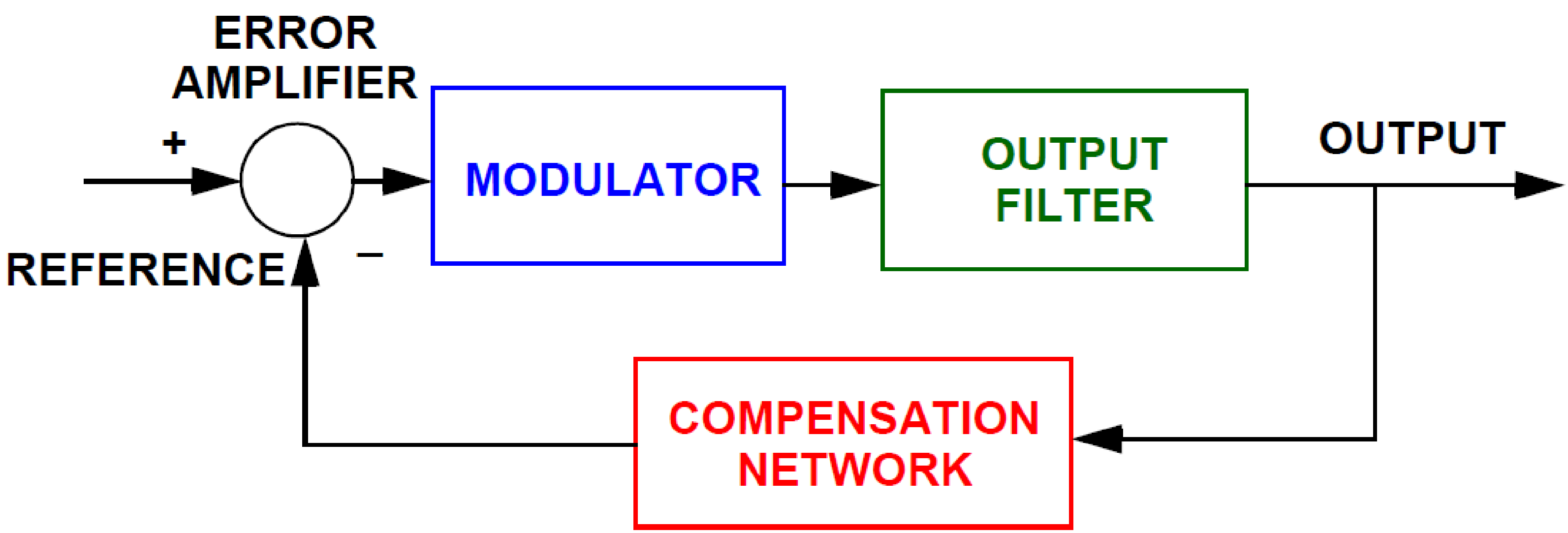
- Voltage Mode
- Current Mode
- Constant on time

Voltage Mode Control

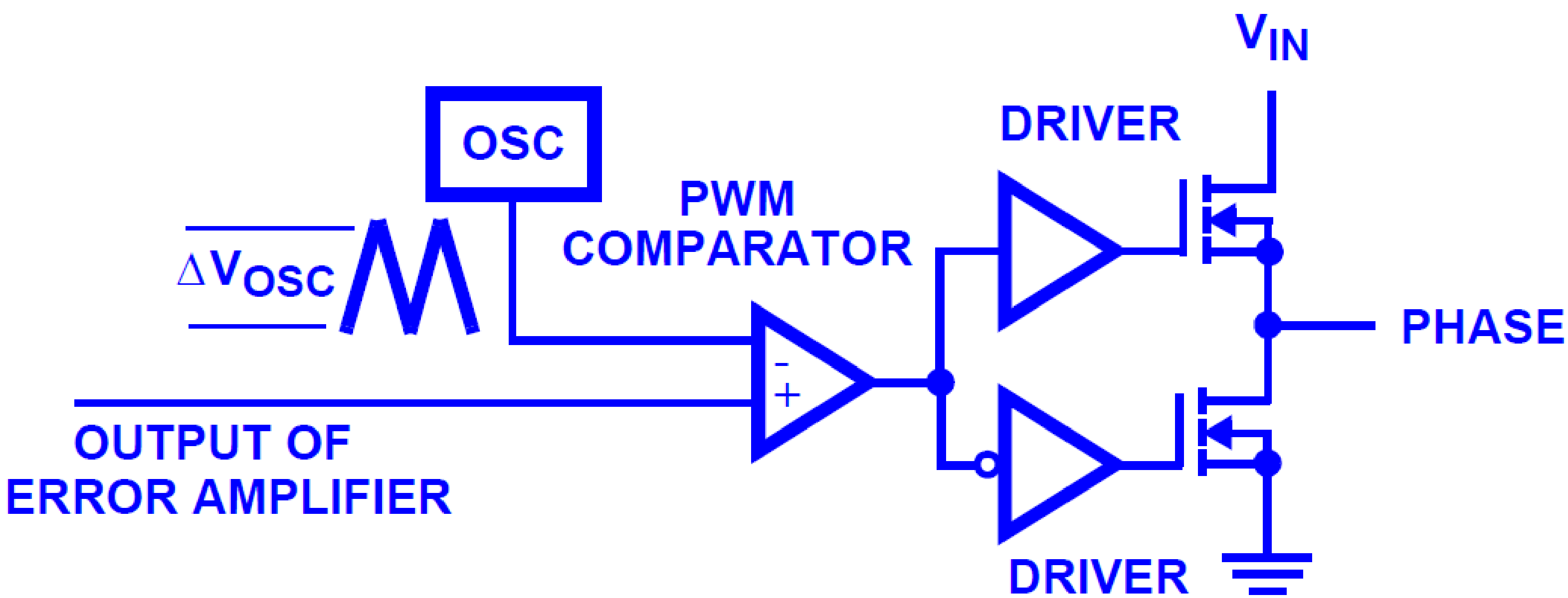




BASIC BLOCKS OF THE BUCK REGULATOR

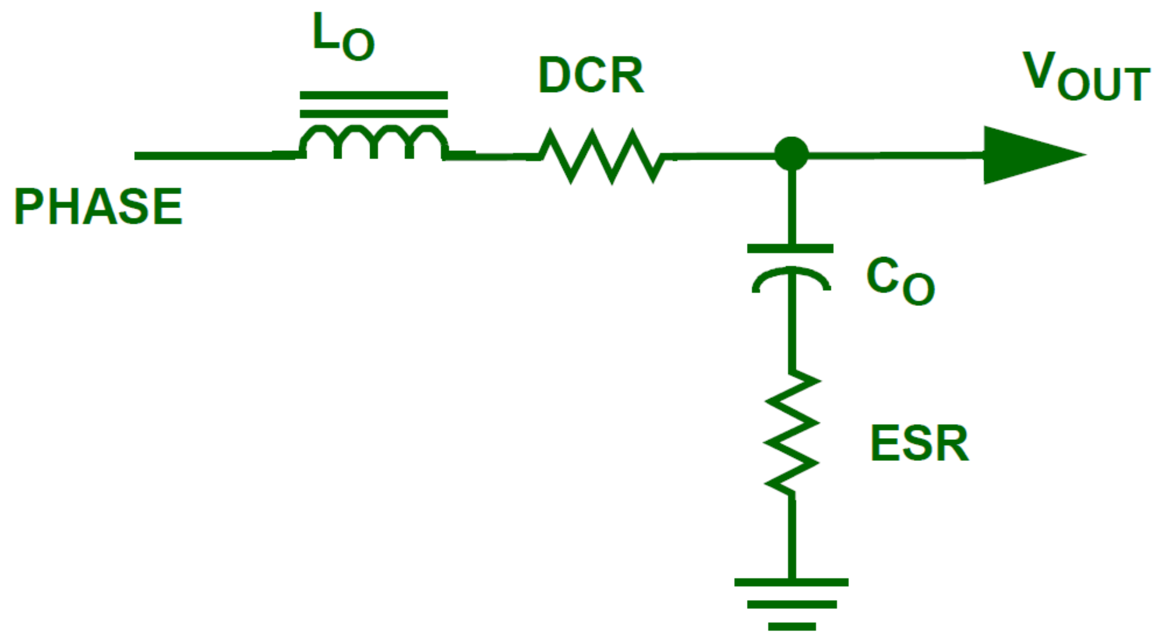


The Modulator



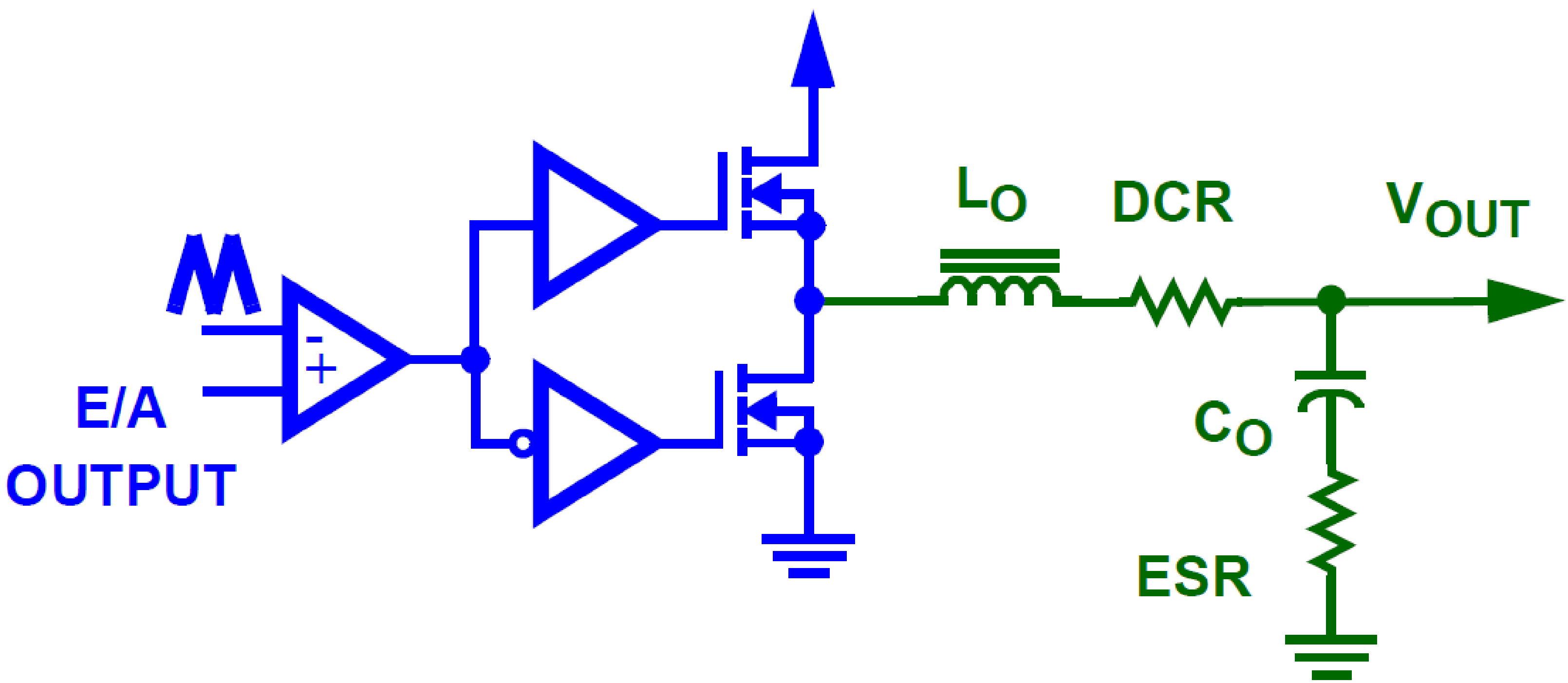
$$GAIN_{MODULATOR} = \frac{V_{IN}}{\Delta V_{OSC}}$$

The Output Filter



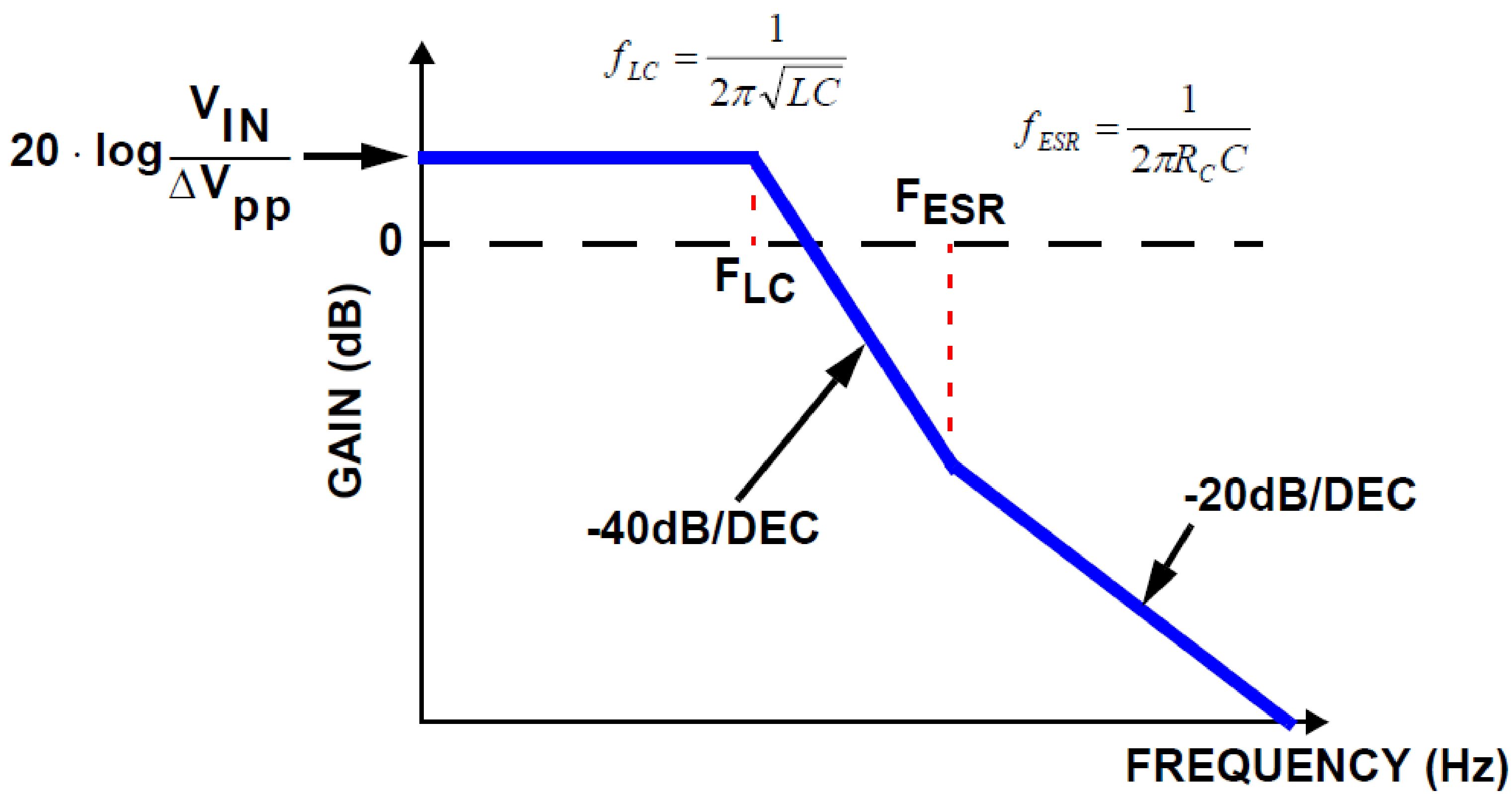
$$GAIN_{FILTER} = \frac{1 + s \cdot ESR \cdot C_{OUT}}{1 + s \cdot (ESR + DCR) \cdot C_{OUT} + s^2 \cdot L_{OUT} \cdot C_{OUT}}$$

The Open Loop System



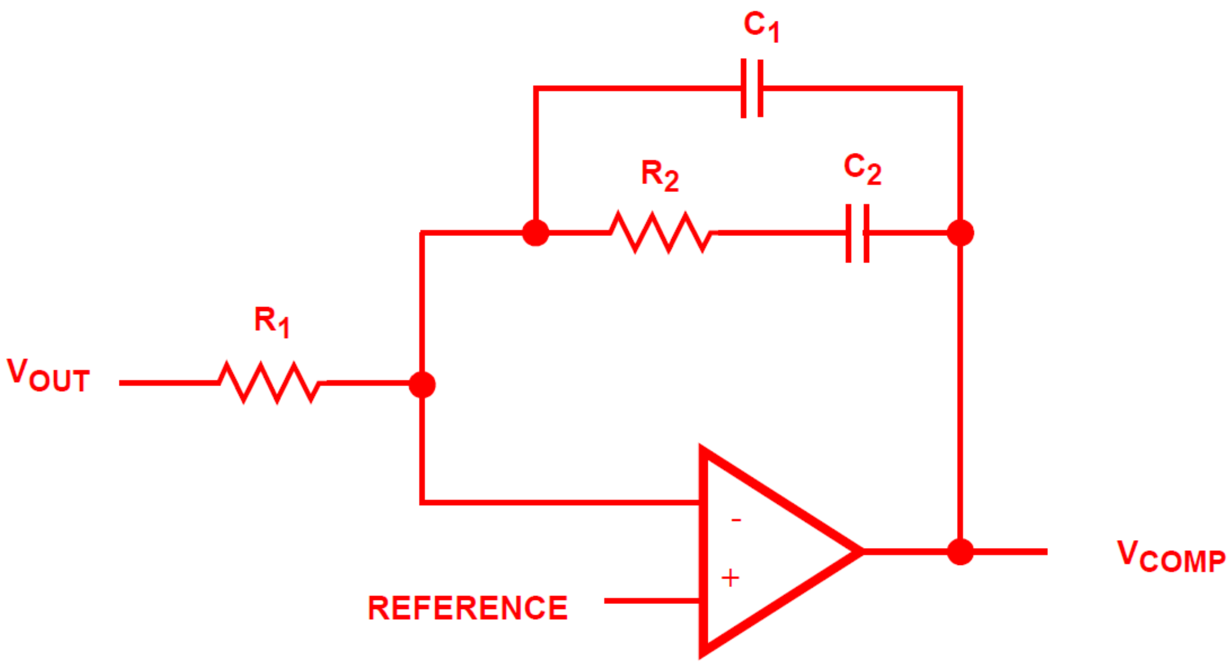
$$GAIN_{OPENLOOP} = \frac{V_{IN}}{\Delta V_{OSC}} \cdot \frac{1 + s \cdot ESR \cdot C_{OUT}}{1 + s \cdot (ESR + DCR) \cdot C_{OUT} + s^2 \cdot L_{OUT} \cdot C_{OUT}}$$

OPEN LOOP SYSTEM GAIN



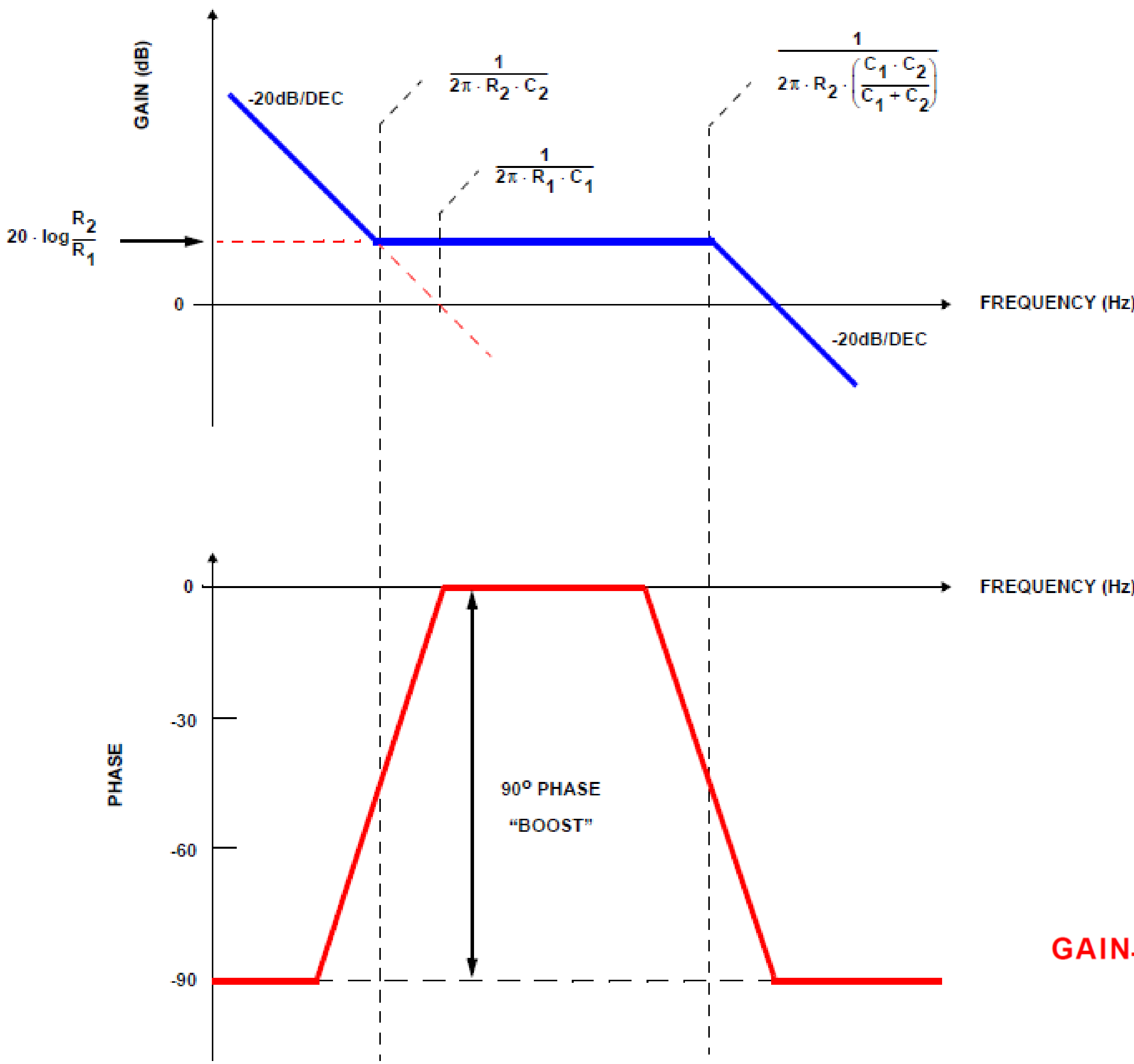
$$GAIN_{OPENLOOP} = \frac{V_{IN}}{\Delta V_{OSC}} \cdot \frac{1 + s \cdot ESR \cdot C_{OUT}}{1 + s \cdot (ESR + DCR) \cdot C_{OUT} + s^2 \cdot L_{OUT} \cdot C_{OUT}}$$

Type II Compensation



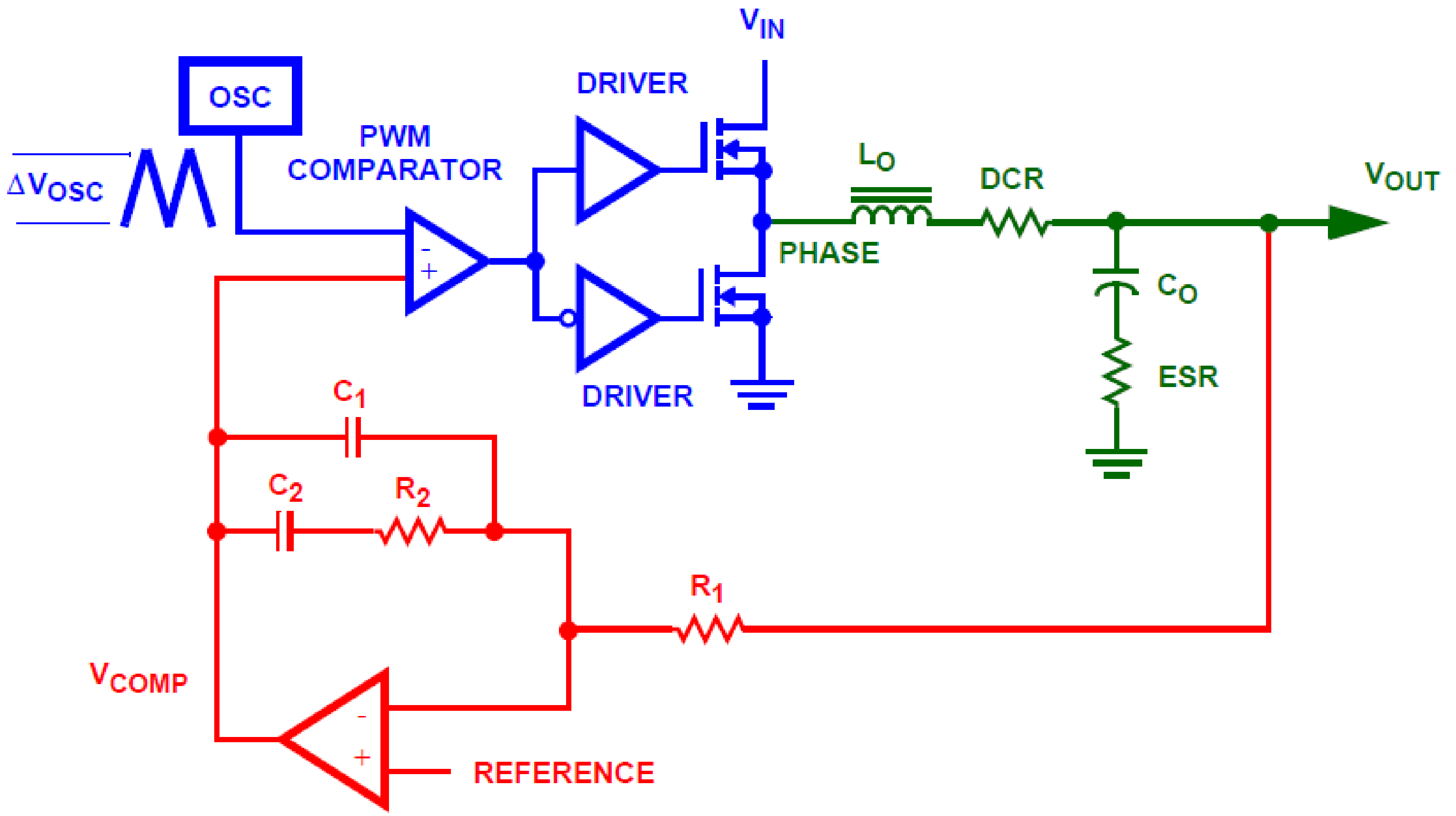
$$GAIN_{TYPEII} = \frac{1}{R_1 \cdot C_1} \cdot \frac{\left(s + \frac{1}{R_2 \cdot C_2}\right)}{s \cdot \left(s + \frac{C_1 + C_2}{R_2 \cdot C_1 \cdot C_2}\right)}$$

Type II Compensation



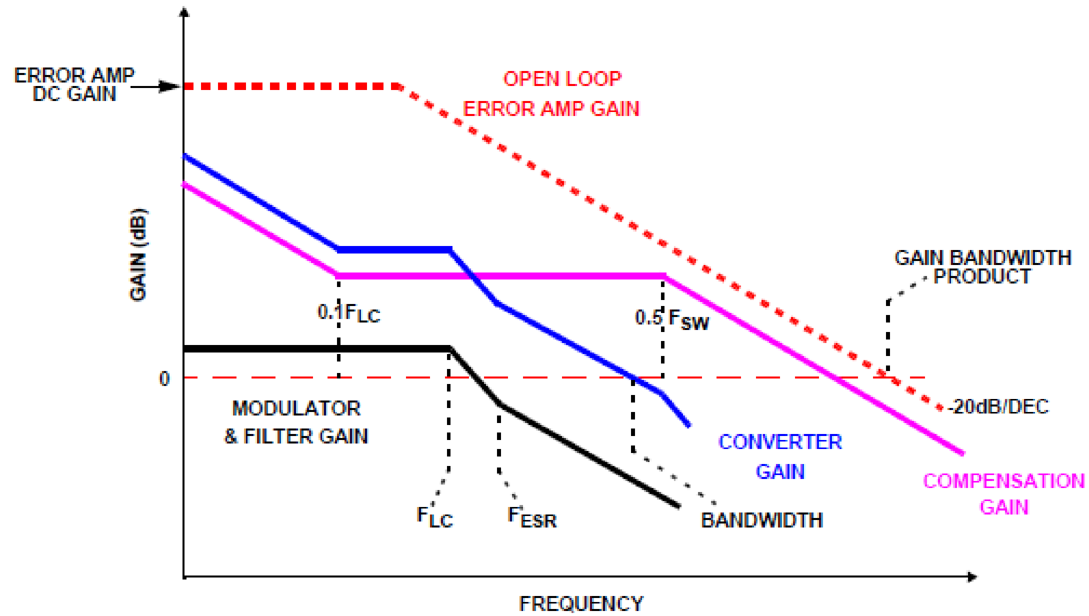
$$GAIN_{TYPEII} = \frac{1}{R_1 \cdot C_1} \cdot \frac{\left(s + \frac{1}{R_2 \cdot C_2}\right)}{s \cdot \left(s + \frac{C_1 + C_2}{R_2 \cdot C_1 \cdot C_2}\right)}$$

Closed Loop System with TYPE II Network



$$GAIN_{SYSTEM} = \frac{1}{R_1 \cdot C_1} \cdot \frac{\left(s + \frac{1}{R_2 \cdot C_2}\right)}{s \cdot \left(s + \frac{C_1 + C_2}{R_2 \cdot C_1 \cdot C_2}\right)} \cdot \frac{V_{IN}}{\Delta V_{OSC}} \cdot \frac{1 + s \cdot ESR \cdot C_{OUT}}{1 + s \cdot (ESR + DCR) \cdot C_{OUT} + s^2 \cdot L_{OUT} \cdot C_{OUT}}$$

TYPE II Compensated Network



$$GAIN_{dB}(f) = GAIN_{MODULATOR} + GAIN_{FILTER} + GAIN_{TYPEII}$$

$$PHASE(f) = PHASE_{MODULATOR} + PHASE_{FILTER} + PHASE_{TYPEII}$$

Where: $GAIN_{MODULATOR} = 20 \cdot \log\left(\frac{V_{IN}}{\Delta V_{OSC}}\right)$

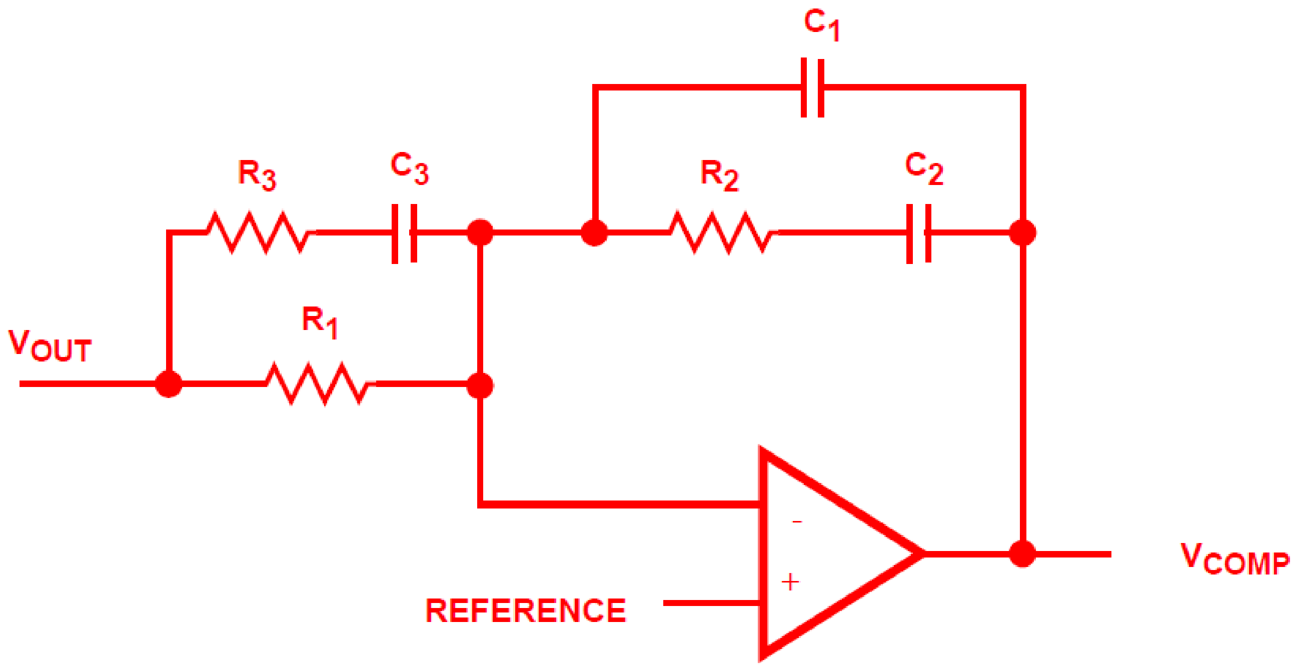
$$GAIN_{FILTER} = 10 \cdot \log\left[1 + (2\pi f \cdot ESR \cdot C_{OUT})^2\right] - 10 \cdot \log\left[\left(1 - (2\pi f)^2 \cdot L_{OUT} \cdot C_{OUT}\right)^2 + (2\pi f \cdot (ESR + DCR) \cdot C_{OUT})^2\right]$$

$$PHASE_{FILTER} = \operatorname{atan}[2\pi f \cdot ESR \cdot C_{OUT}] + \operatorname{atan}\left[\frac{2\pi f \cdot ESR + DCR \cdot C_{OUT}}{2\pi f^2 \cdot L_{OUT} \cdot C_{OUT} - 1}\right]$$

$$GAIN_{TYPEII} = 10 \cdot \log\left[1 + (2\pi f \cdot R_2 \cdot C_2)^2\right] - 20 \cdot \log[2\pi f \cdot R_1 \cdot (C_1 + C_2)] - 10 \cdot \log\left[1 + \left(2\pi f \cdot R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)\right)^2\right]$$

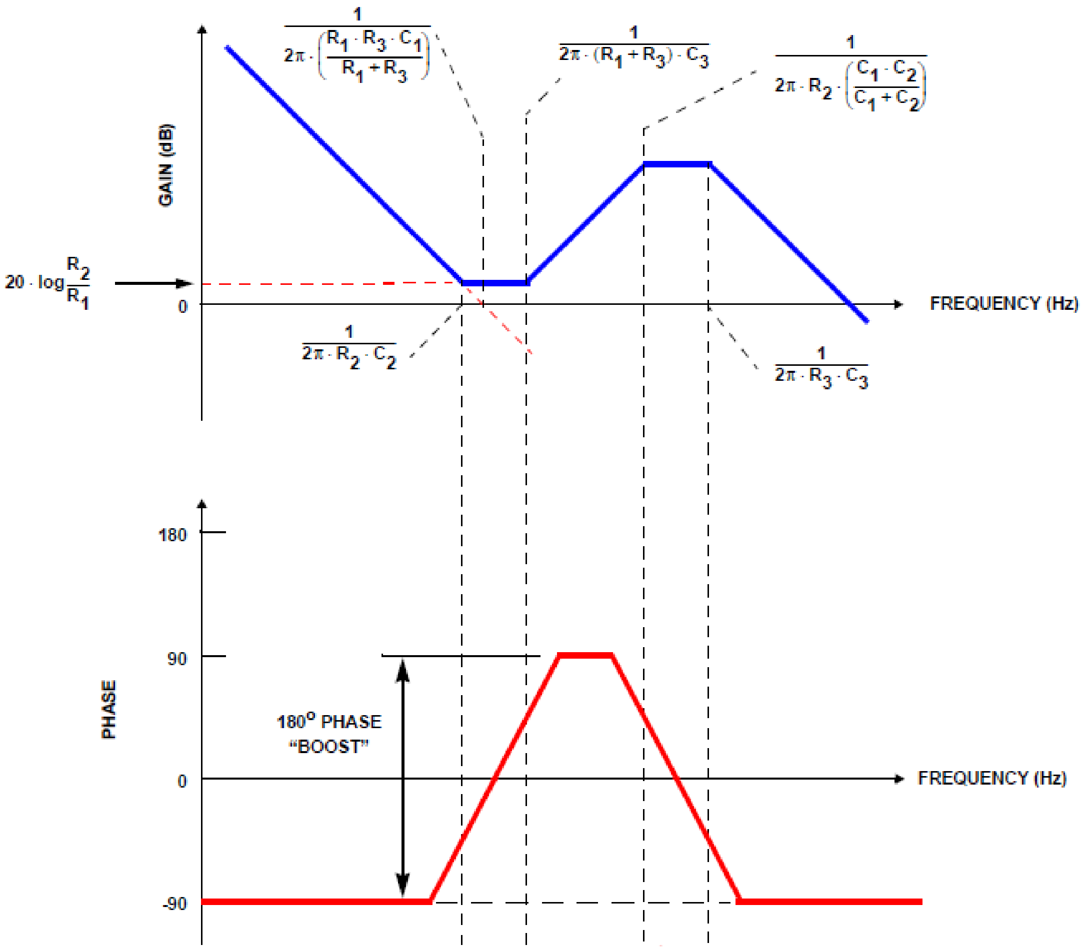
$$PHASE_{TYPEII} = -90^{o} + \operatorname{atan}[2\pi f \cdot R_2 \cdot C_2] - \operatorname{atan}\left[2\pi f \cdot R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)\right]$$

Generic TYPE III Network

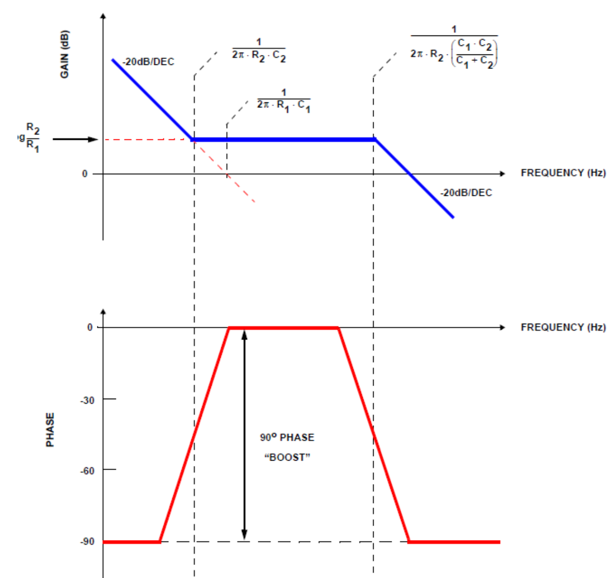


$$GAIN_{TYPEIII} = \frac{R_1 + R_3}{R_1 \cdot R_3 \cdot C_1} \cdot \frac{\left(s + \frac{1}{R_2 \cdot C_2}\right) \cdot \left(s + \frac{1}{(R_1 + R_3) \cdot C_3}\right)}{s \cdot \left(s + \frac{C_1 + C_2}{R_2 \cdot C_1 \cdot C_2}\right) \cdot \left(s + \frac{1}{R_3 \cdot C_3}\right)}$$

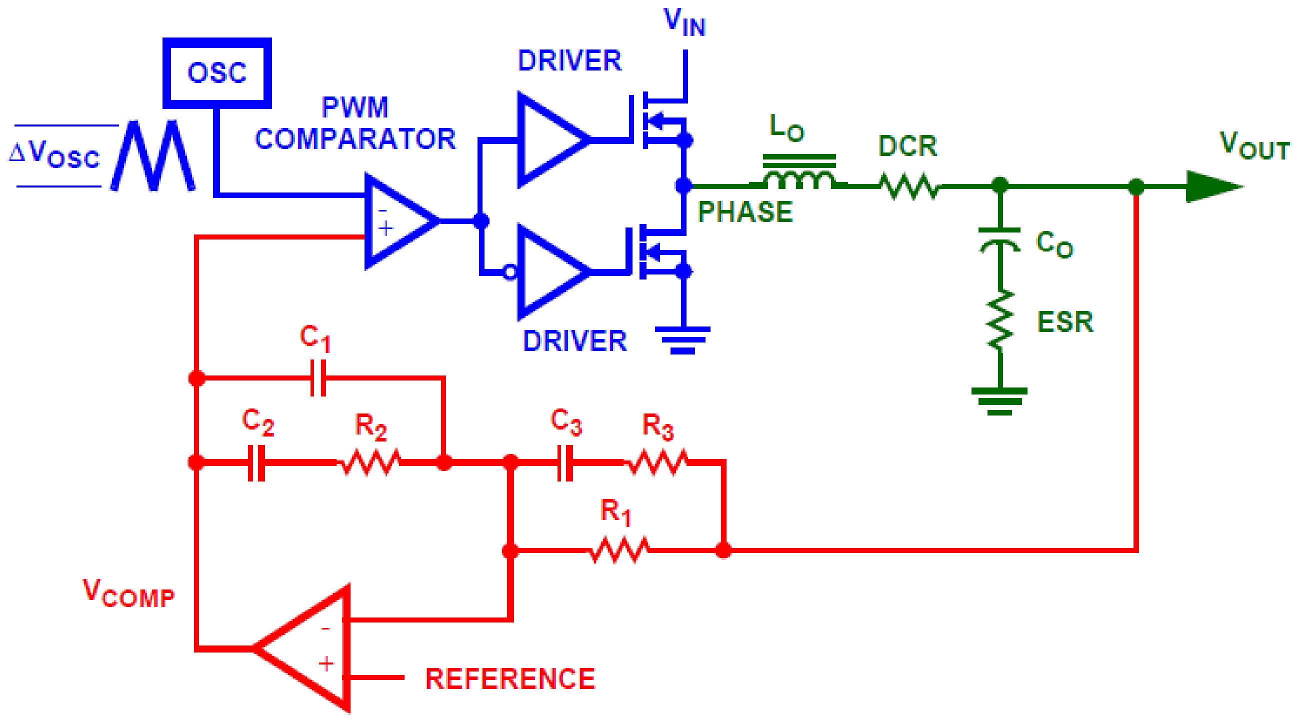
Generic TYPE III Network



$$GAIN_{TYPEIII} = \frac{R_1 + R_3}{R_1 \cdot R_3 \cdot C_1} \cdot \frac{\left(s + \frac{1}{R_2 \cdot C_2}\right) \cdot \left(s + \frac{1}{(R_1 + R_3) \cdot C_3}\right)}{s \cdot \left(s + \frac{C_1 + C_2}{R_2 \cdot C_1 \cdot C_2}\right) \cdot \left(s + \frac{1}{R_3 \cdot C_3}\right)}$$

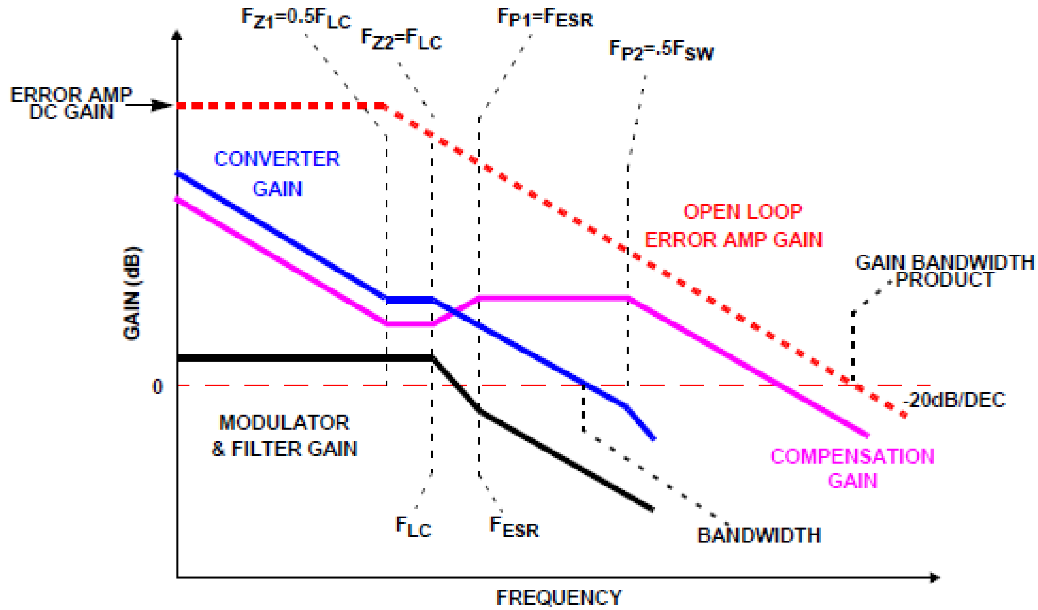


Closed Loop System with TYPE III Network



$$GAIN_{SYSTEM} = \frac{R_1 + R_3}{R_1 \cdot R_3 \cdot C_1} \cdot \frac{\left(s + \frac{1}{R_2 \cdot C_2}\right) \cdot \left(s + \frac{1}{(R_1 + R_3) \cdot C_3}\right)}{s \cdot \left(s + \frac{C_1 + C_2}{R_2 \cdot C_1 \cdot C_2}\right) \cdot \left(s + \frac{1}{R_3 \cdot C_3}\right)} \cdot \frac{V_{IN}}{\Delta V_{OSC}} \cdot \frac{1 + s \cdot ESR \cdot C_{OUT}}{1 + s \cdot (ESR + DCR) \cdot C_{OUT} + s^2 \cdot L_{OUT} \cdot C_{OUT}}$$

TYPE III Compensated Network



$$GAIN_{dB}(f) = GAIN_{MODULATOR} + GAIN_{FILTER} + GAIN_{TYPEIII}$$

$$PHASE(f) = PHASE_{MODULATOR} + PHASE_{FILTER} + PHASE_{TYPEIII}$$

Where: $$GAIN_{MODULATOR} = 20 \cdot \log\left(\frac{V_{IN}}{\Delta V_{OSC}}\right)$$

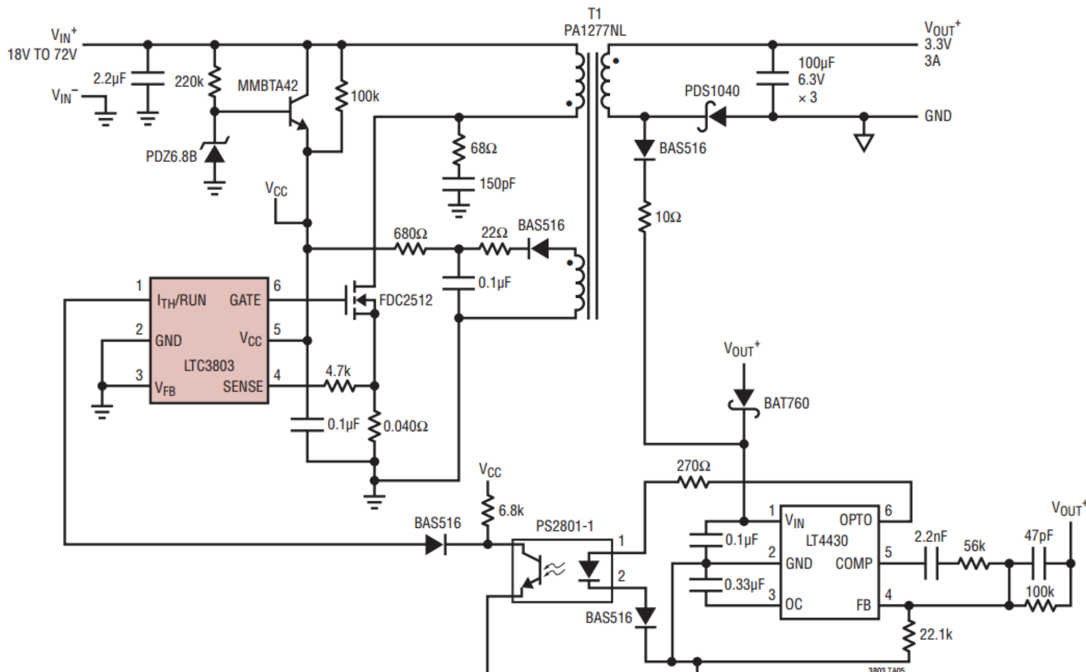
$$GAIN_{FILTER} = 10 \cdot \log\left[1 + (2\pi f \cdot ESR \cdot C_{OUT})^2\right] - 10 \cdot \log\left[\left(1 - (2\pi f)^2 \cdot L_{OUT} \cdot C_{OUT}\right)^2 + (2\pi f \cdot (ESR + DCR) \cdot C_{OUT})^2\right]$$

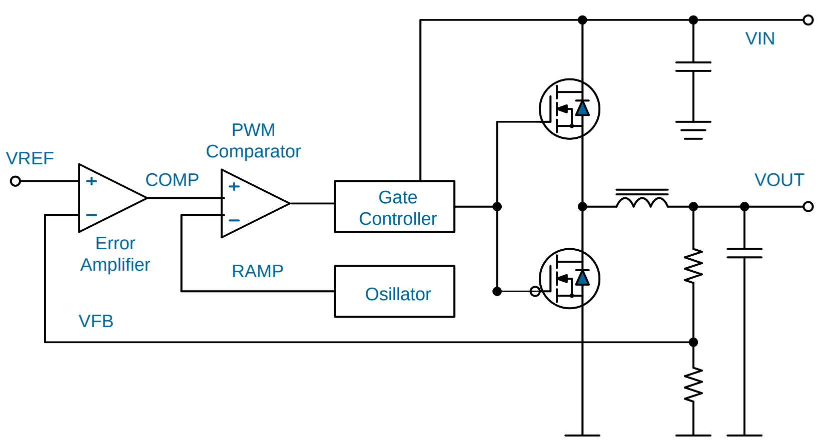
$$PHASE_{FILTER} = \operatorname{atan}[2\pi f \cdot ESR \cdot C_{OUT}] + \operatorname{atan}\left[\frac{2\pi f \cdot ESR + DCR \cdot C_{OUT}}{2\pi f^2 \cdot L_{OUT} \cdot C_{OUT} - 1}\right]$$

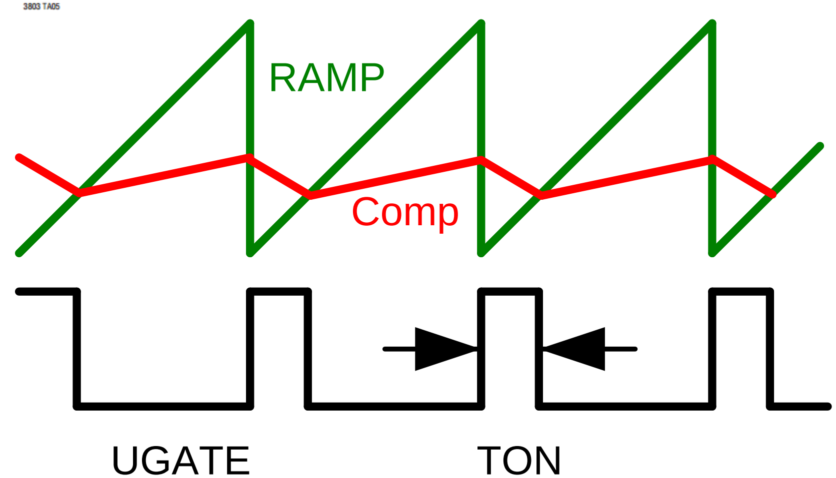
$$GAIN_{TYPEIII} = 10 \cdot \log\left[1 + (2\pi f \cdot R_2 \cdot C_2)^2\right] - 20 \cdot \log[2\pi f \cdot R_1 \cdot (C_1 + C_2)] - 10 \cdot \log\left[1 + \left(2\pi f \cdot R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)\right)^2\right] + 10 \cdot \log\left[1 + (2\pi f \cdot (R_1 + R_3) \cdot C_3)^2\right] - 10 \cdot \log\left[1 + (2\pi f \cdot R_3 \cdot C_3)^2\right]$$

$$PHASE_{TYPEIII} = -90^o + \operatorname{atan}[2\pi f \cdot R_2 \cdot C_2] - \operatorname{atan}\left[2\pi f \cdot R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)\right] + \operatorname{atan}[2\pi f \cdot (R_1 + R_3) \cdot C_3] - \operatorname{atan}[2\pi f \cdot R_3 \cdot C_3]$$

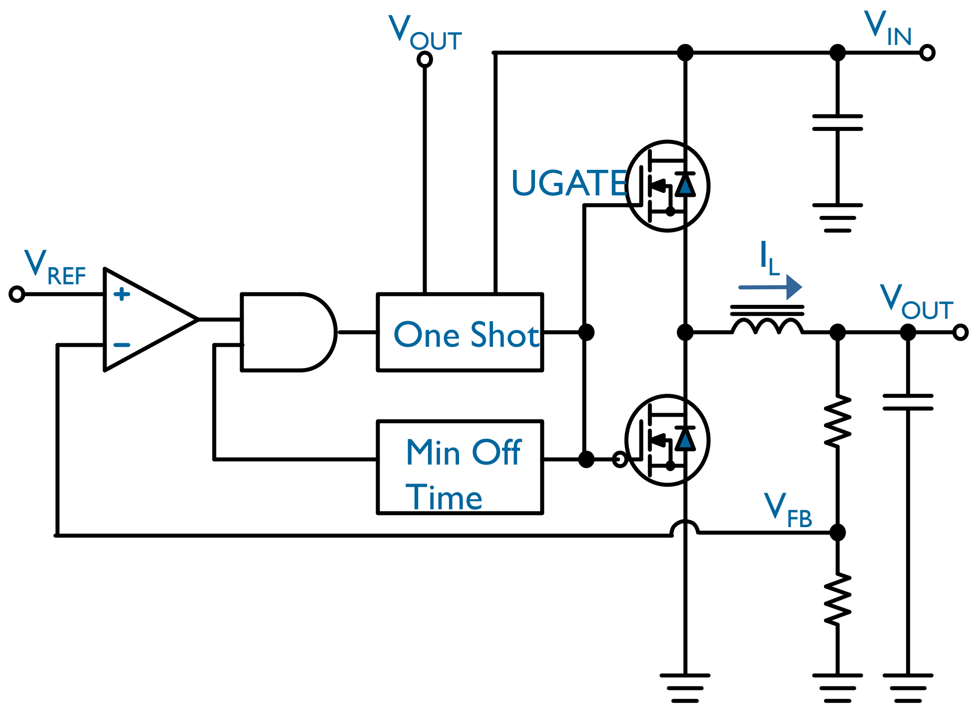
Current Mode Control

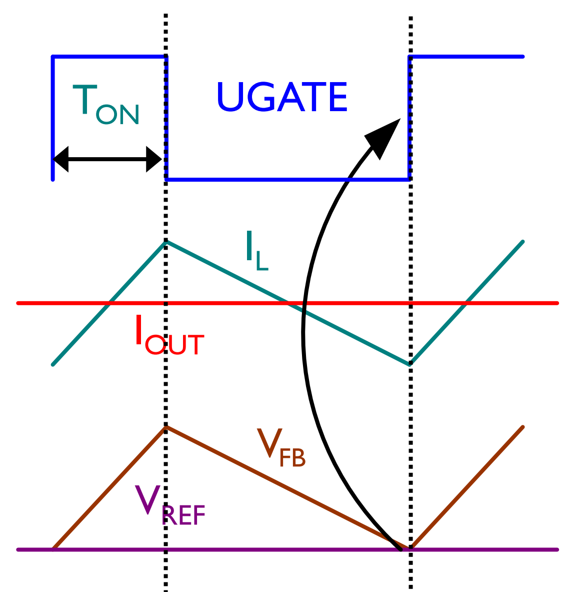




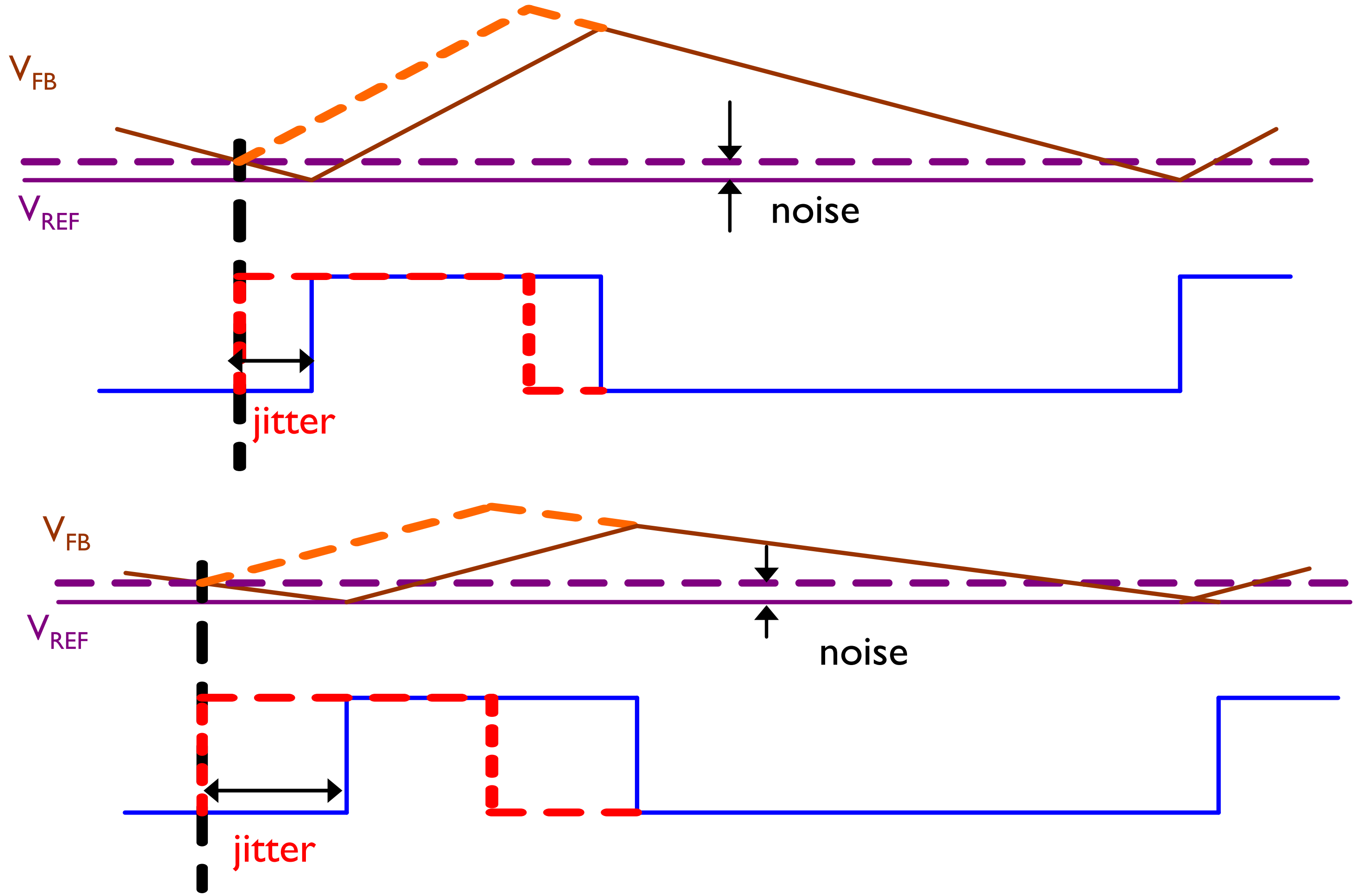


Constant On Time Control

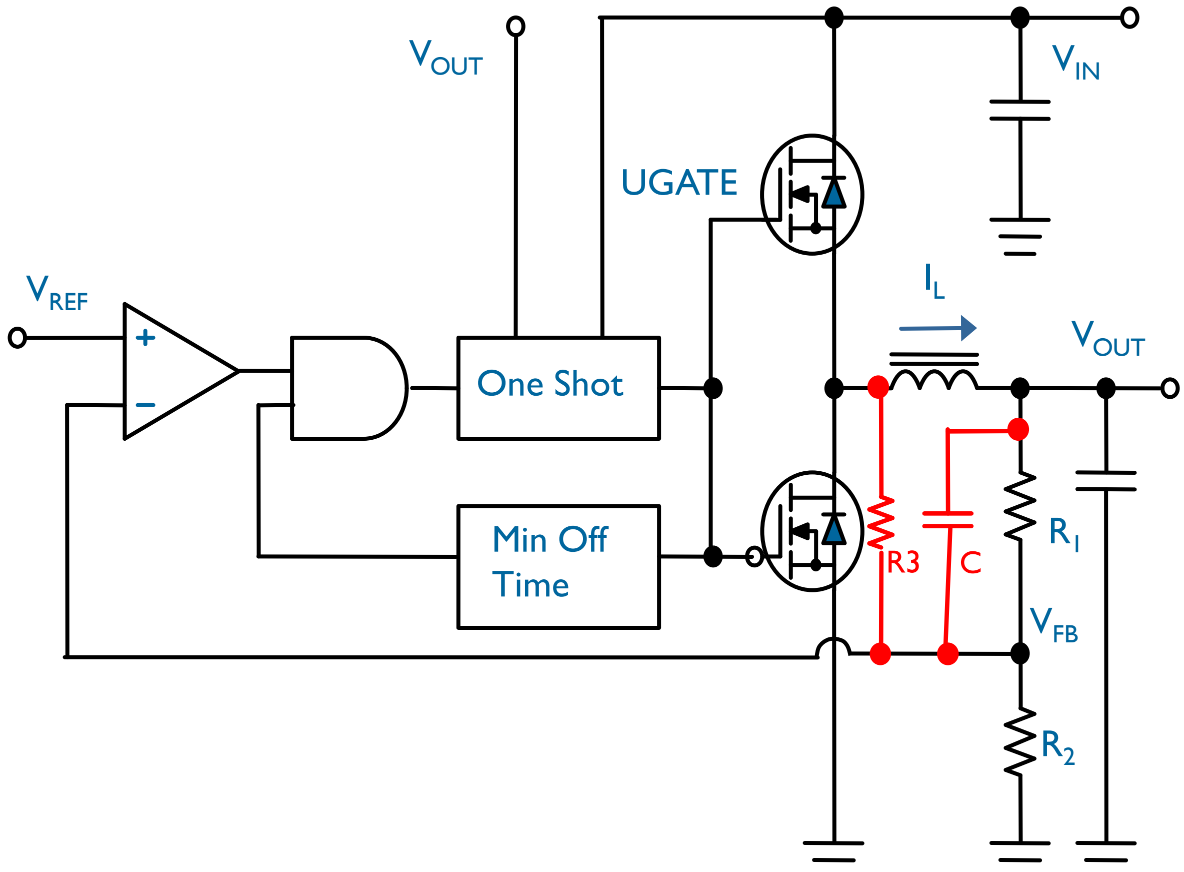




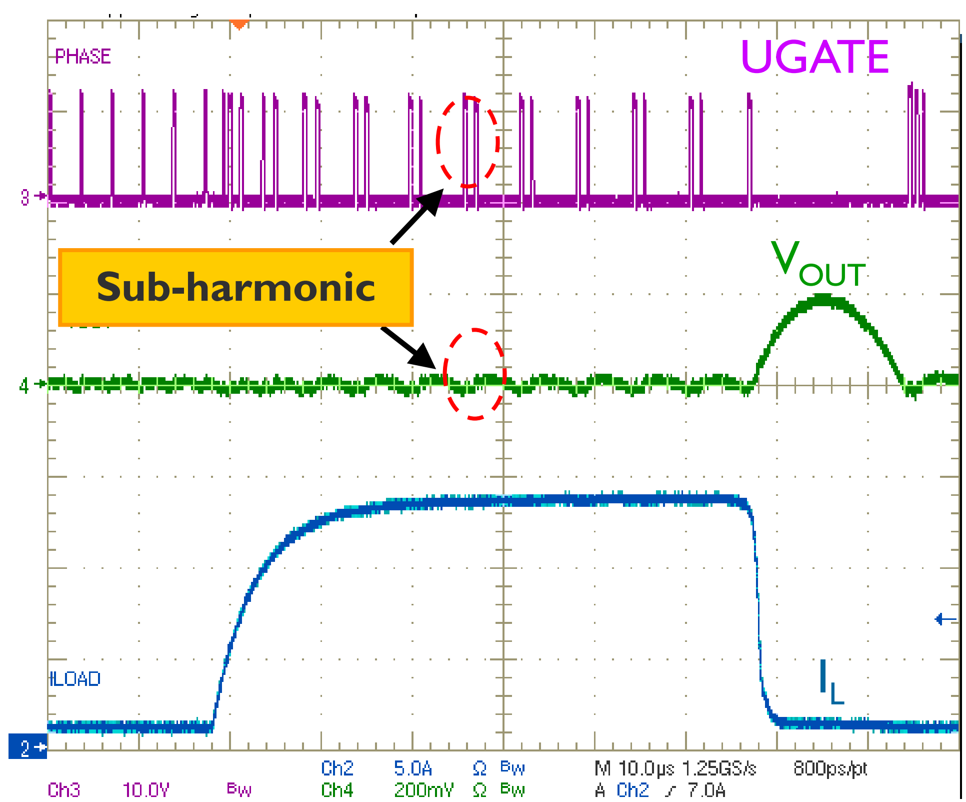
Constant On Time Control-Jitter



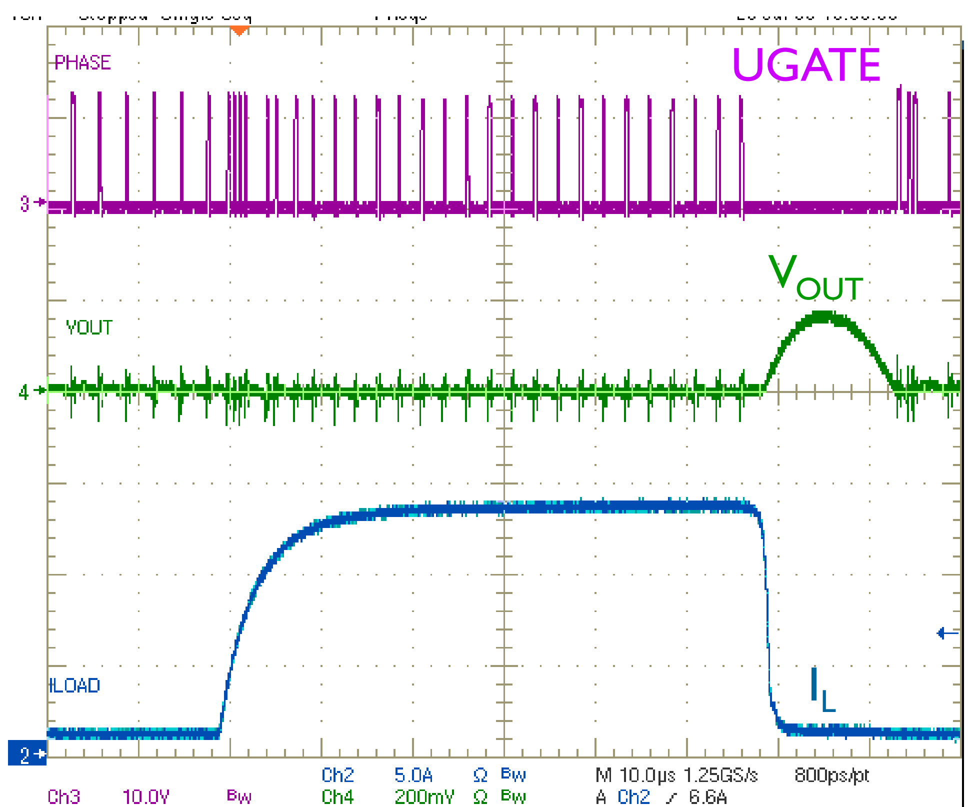
Constant On Time Control-Jitter



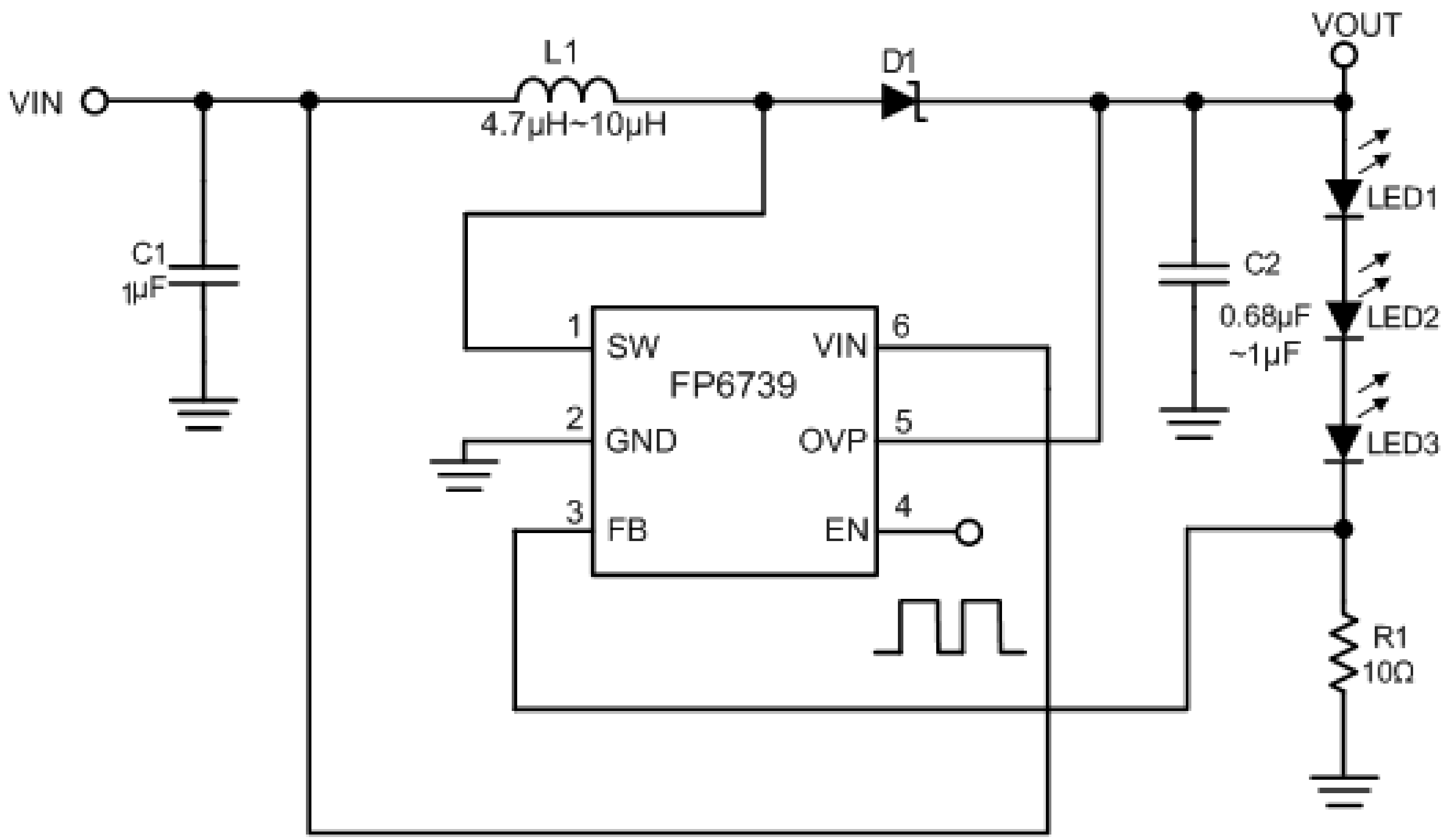
Constant On Time Control-Jitter



Constant On Time Control-Jitter



LED Driver



VIN
L1
4.7µH~10µH
D1
VOUT
C1
1µF
LED1
C2
0.68µF
~1µF
LED2
LED3
1
SW
6
VIN
FP6739
2
GND
5
OVP
3
FB
4
EN
R1
10Ω

Thanks You!