National Cheng Kung University
Graduate Institute of Electrical Engineering
Communication and Biologic Integrated Circuit

2015 NFU Seminar

穿戴式電路、系統與應用

應用=>系統=>電路

Shuenn-Yuh Lee
EE / NCKU
Taiwan

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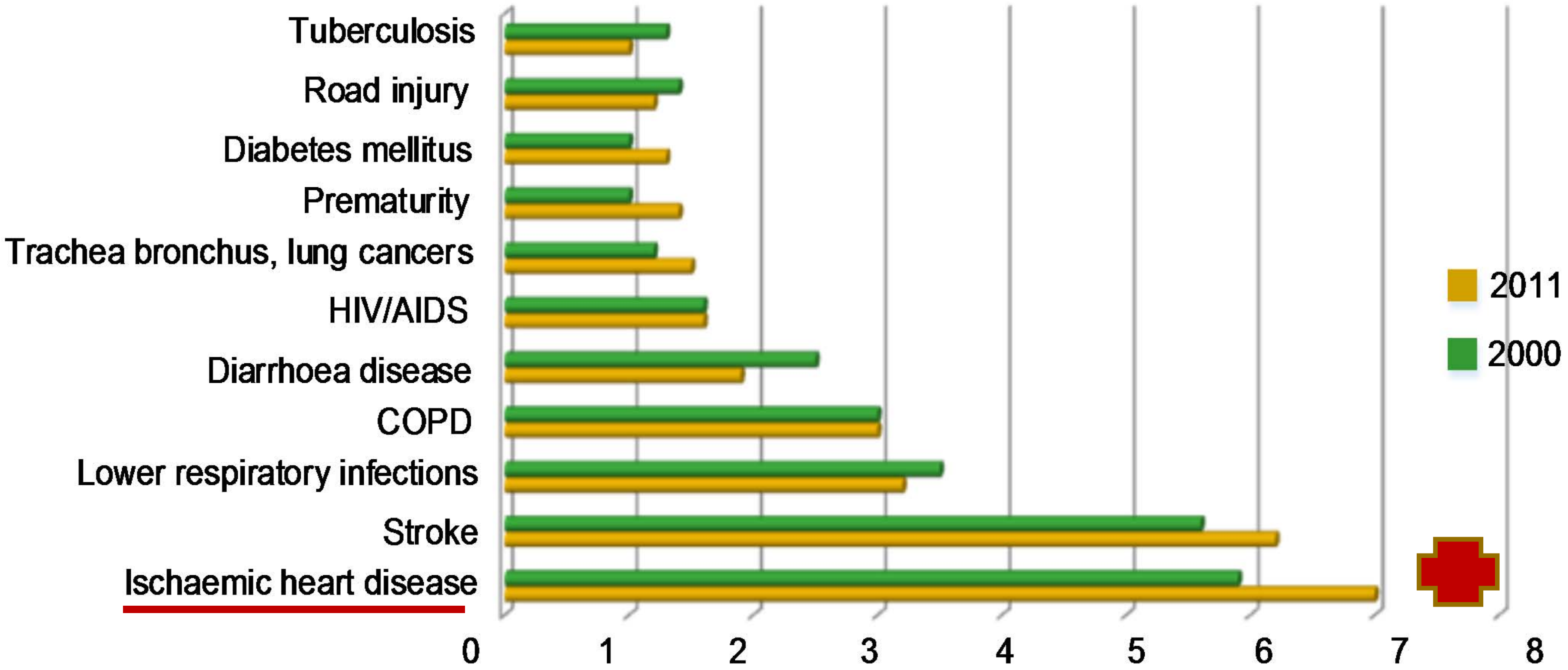
Communication and Biologic
Integrated Circuit Lab

Outline

- **Introduction of out-of-body sensor networks for Interactive Intelligent Healthcare and Monitoring System (IIHMS)**
- A low-power wireless ECG acquisition circuit and system for body sensor networks
- A wireless ECG acquisition SoC with ZigBee System

Motivation: Top Ten Causes of Death [1]

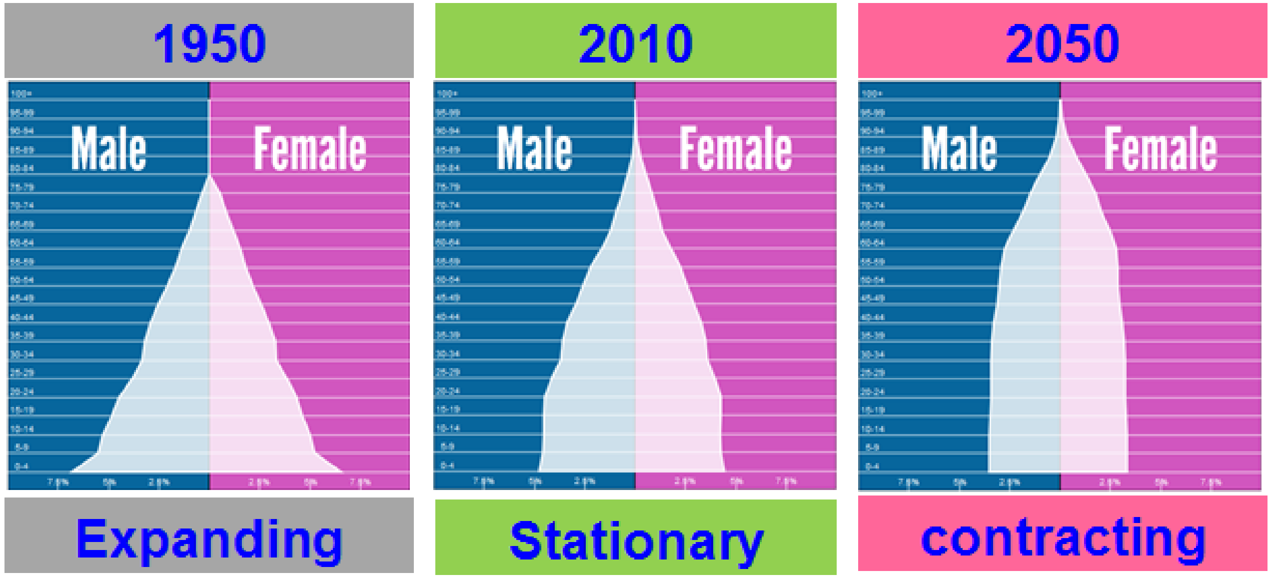


Unit: millions people

[1] http://www.who.int/mediacentre/factsheets/fs310/en/index.html

Motivation: Population Pyramid

- In the past and prediction [2]
  - Population: 2.51@1950s, 6.89@2010s, 9.31@2050s (billions)

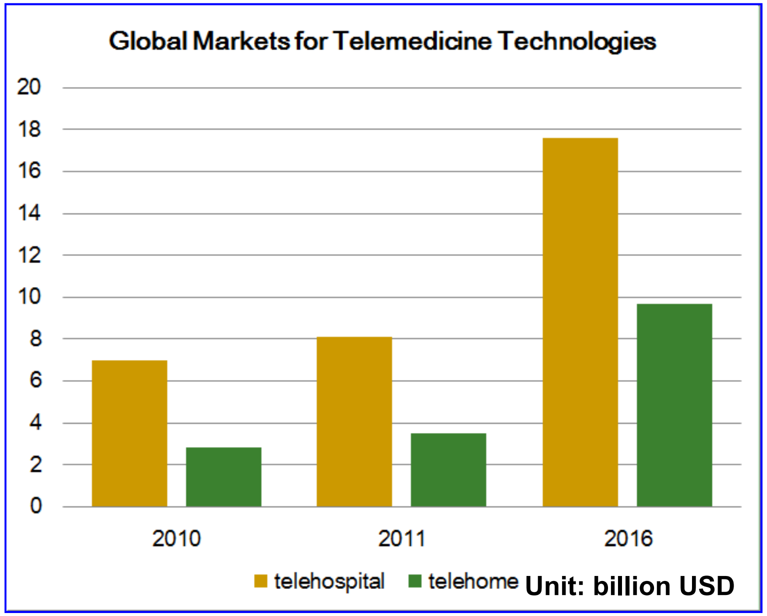


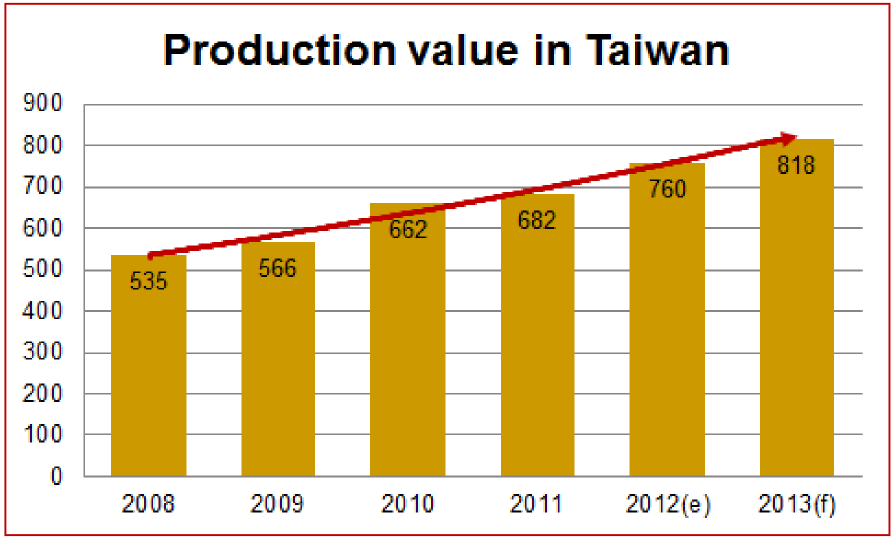
- Old age population ratio ↑, young age population ratio ↓
  - Elders have higher risk of diseases. [3]
  - Labor force ↓, elderly care requirement ↑

[2] http://populationpyramid.net/
[3] http://www.cdc.gov/heartdisease/statistical_reports.htm

Motivation: Market Issue

- Global markets for telemedicine technologies [4]
- Medical devices production value in Taiwan [5]
- APAC's Medical Devices Market [6]





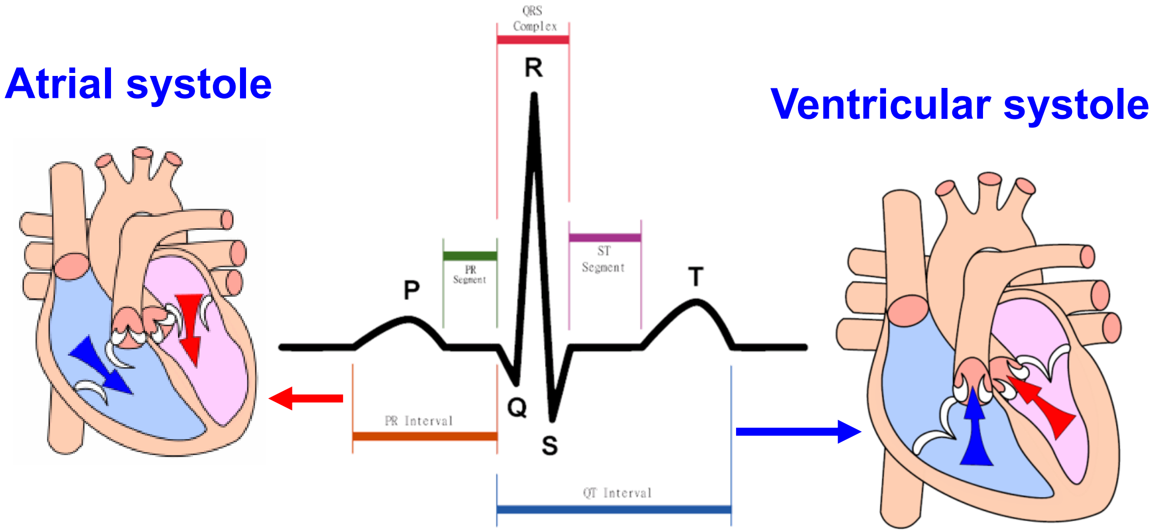
Unit: billion NTD

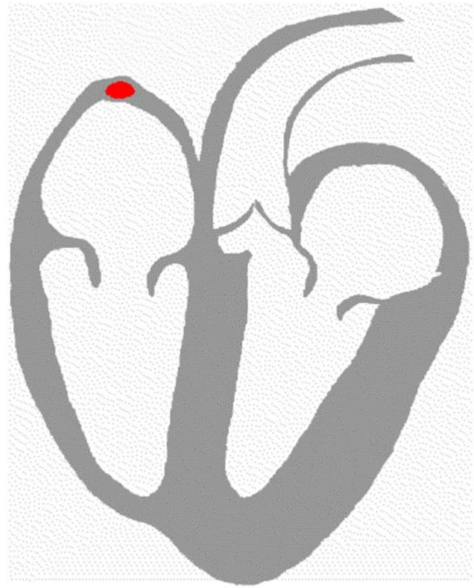
- **Production value of medical devices ↑ every year in the world**

[4] http://www.bccresearch.com/market-research/healthcare/telemedicine-technologies-global-markets-hlc014e.html
[5] http://www.medicaretaiwan.com/zh_TW/news/info.html?id=AD9CC42D0785C1A4
[6] http://www.slideshare.net/FrostandSullivan/frost-sullivan-apacs-medical-devices-market-ready-to-skyrocket

Motivation: Current Products

- For the heart disease monitoring
  - Products
    - iMEC [7]: ECG patch
    - iRhythm [8]: Zio® patch
    - XinBo [9][10]: ECG patch

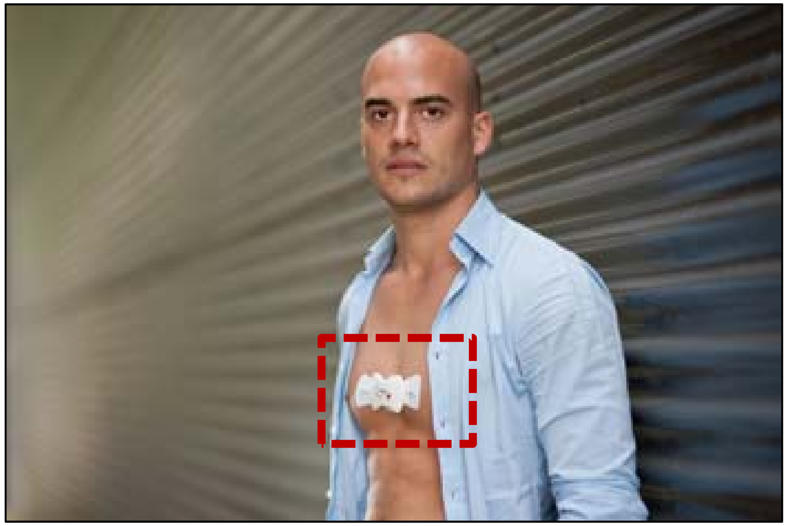




[7] http://www2.imec.be/be_en/home.html
[8] http://www.irhythmtech.com
[9] T.B.J. Kuo, "Electrocardiogram signal collecting apparatus," US patent 6-360-117 B1, Mar. 19, 2002.
[10] https://itri.org.tw/chi/tech-transfer/04.asp?RootNodeId=040&NodeId=041&id=4424

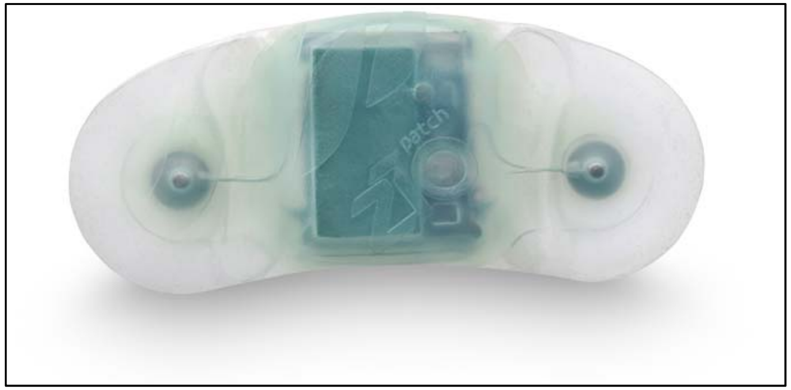
Current Products (1/2)

iMEC [7]: ECG patch



- Physical activity monitoring
  - 3-lead ECG signals
  - Tissue-contact impedance
  - 3D-accelerometer
- Wireless transmission (BLE)
- One week

iRhythm [8]: Zio® patch



- 1-lead ECG signals
- Off-line recording
- higher diagnostic yield
- Two weeks
- recyclable

Current Products (2/2)

Xinbo [9]: ECG patch

- ECG & heart rate variability (HRV) detection
  - One lead
  - Bandwidth: 250Hz
  - Resolution: 8 bits
- Wireless transmission (Xenon RF module)
- One day (with one CR2032 battery, 3V & 230 mAh)
- Integrated into the rehabilitation platform (ITRI: Industrial Technology Research Institute of Taiwan) [10]

Wearable Devices for Heart Rate Detection

Phyode WMe Smart Wristband
智慧樂活健康手環

MIO Link
連續心率監測手環

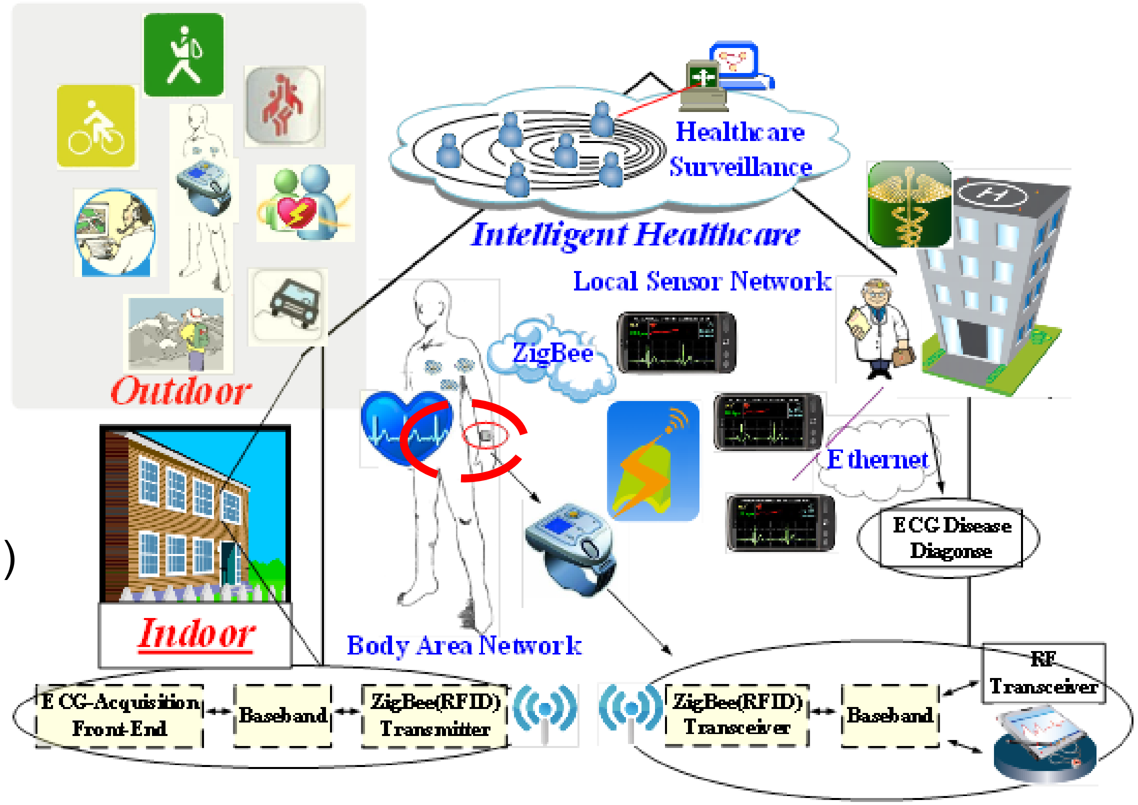
Jawbone UP
時尚智慧手環

Challenges

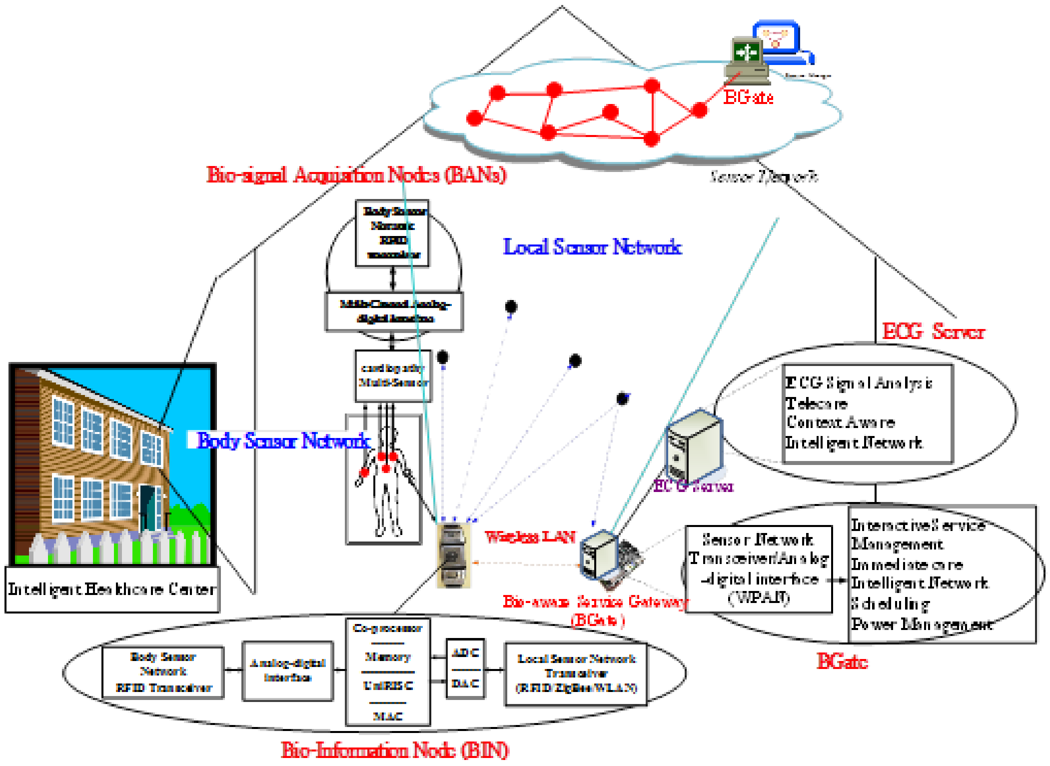
- Home-care system
- Long-term usage
  - Low-power consumption
- Convenient usage
  - Wireless transmission
- High resolution
  - For diagnosing precisely
- Diagnosis
  - For both user and doctor

Interactive Intelligent Healthcare System

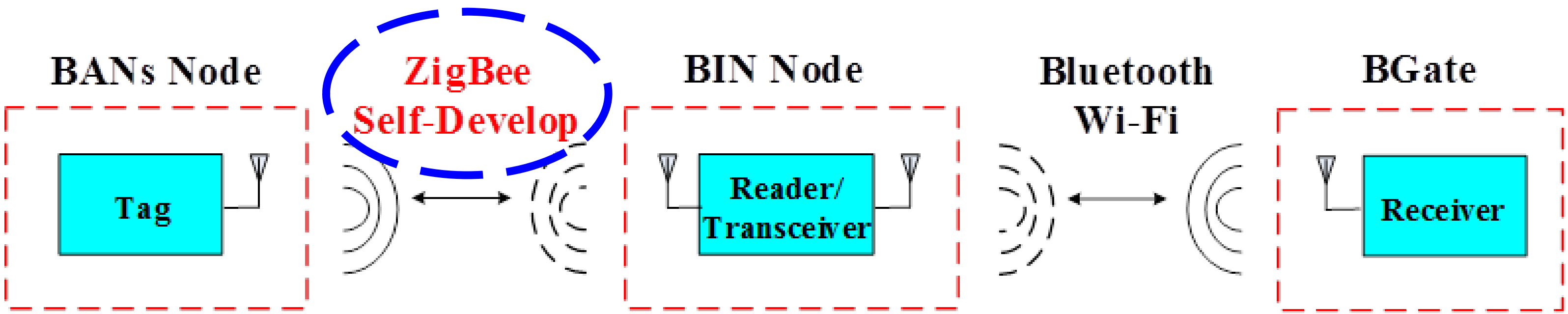
- Targets
  - Low power,
  - Anywhere,
  - Anytime,
  - Long-term monitoring
- Body Area Network
  - Near-body application
  - Acquisition node
    - Wearable device (watch)
- Local Sensor Network
  - Intermediate interface
  - Wearable device
    - Portable facility (PDA)



Heterogeneous Networks For Healthcare Monitoring

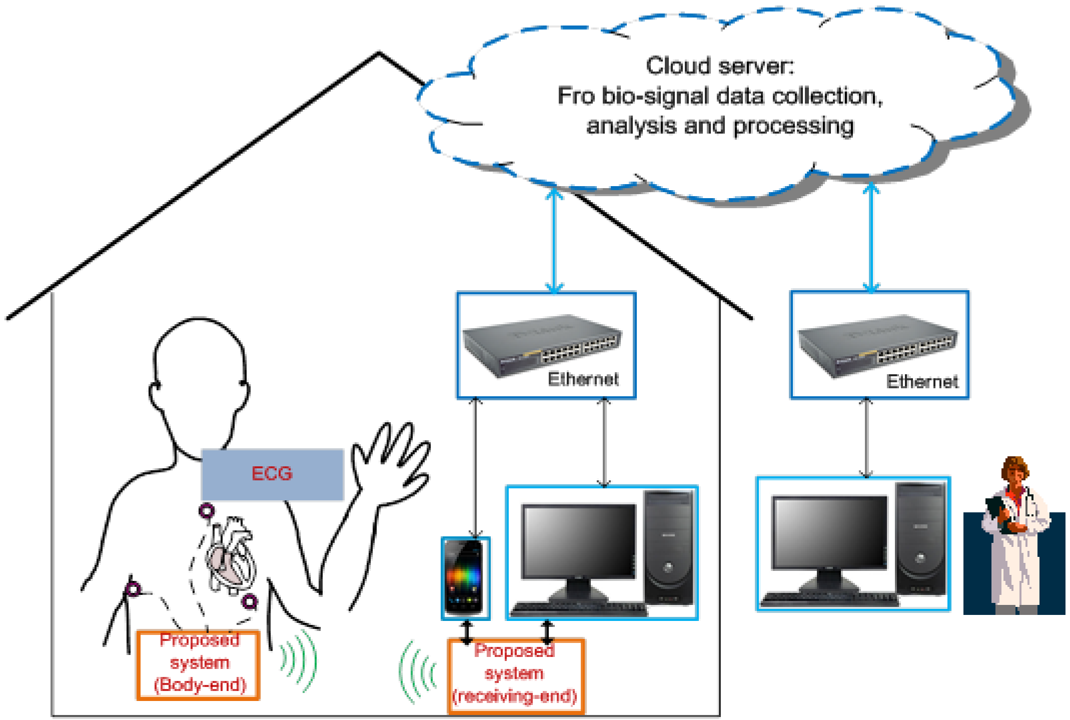


- 3B Concept
  - BAN: Bio-Signal Acquisition Node
  - BIN: Bio-Information Node
  - BGate: Bio-aware Service Gateway
- BAN-BIN
  - ZigBee System
  - Self Developed System
- BIN-BGate
  - Bluetooth
  - Wi-Fi

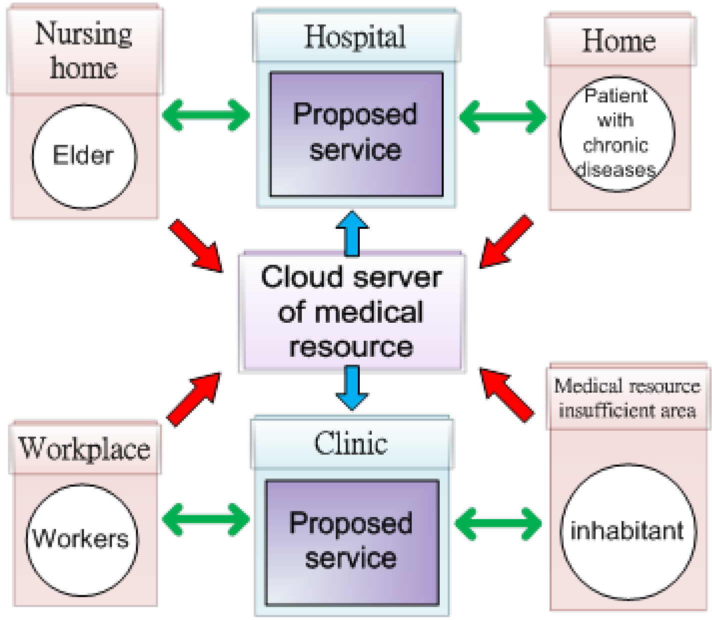


Scenario

Usage scenario



Applications

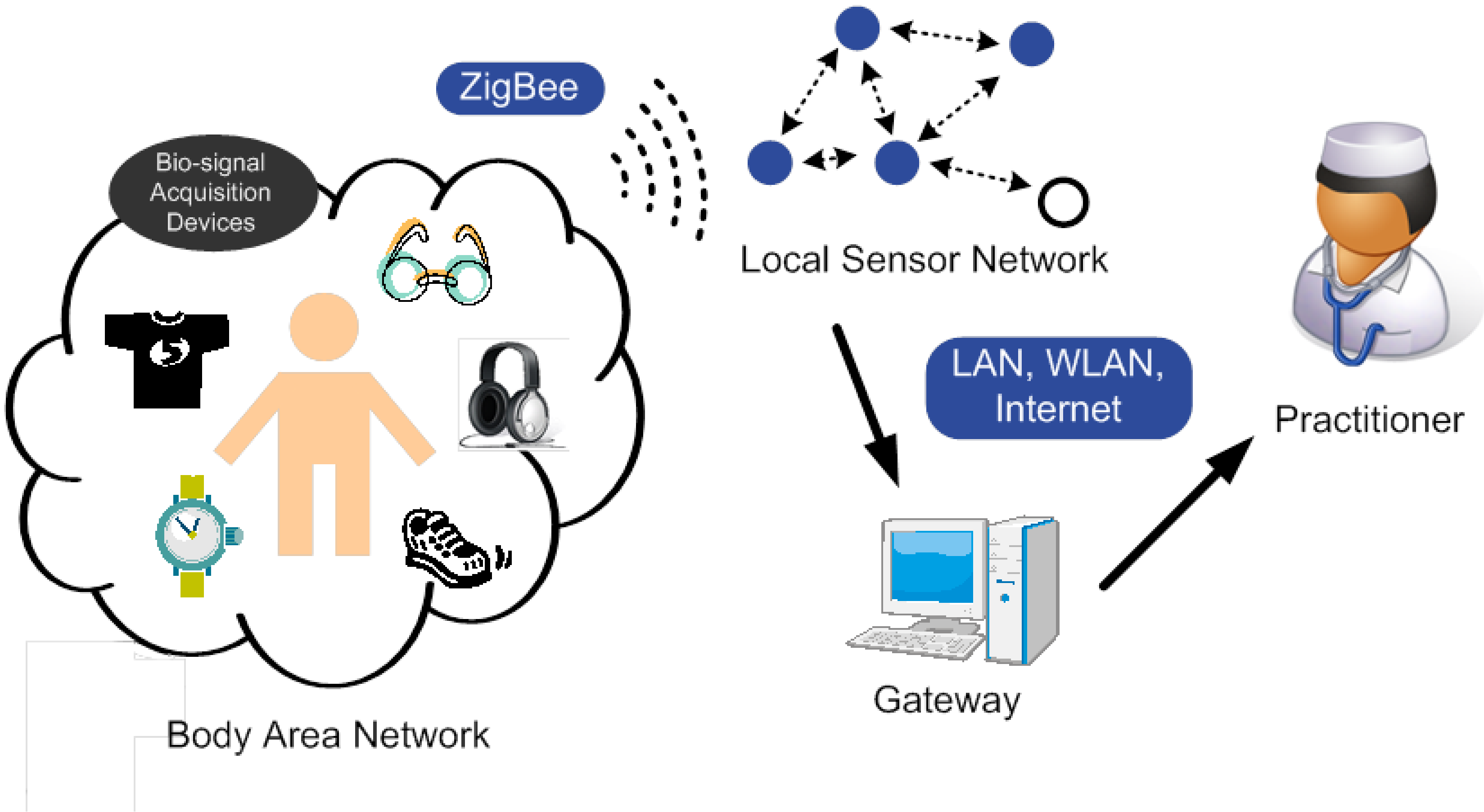


Outline

- Introduction of out-of-body sensor networks for Interactive Intelligent Healthcare and Monitoring System (IIHMS)
- **A low-power wireless ECG acquisition circuit and system for body sensor networks**
- **A wireless ECG acquisition SoC with ZigBee System**

A Wireless ECG Acquisition SoC for ZigBee Applications

- Scenario: Personal Healthcare System



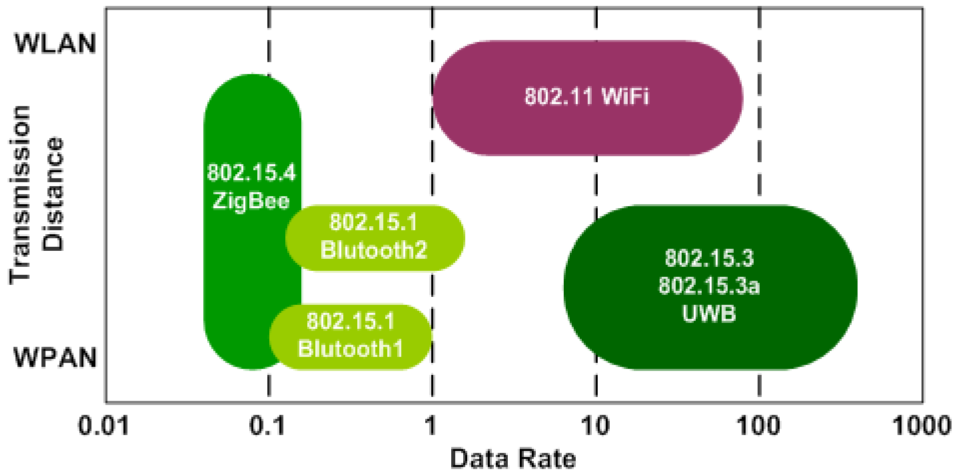
IEEE 802.15.4 Specification (ZigBee)

- Benefits: (Compared with WiFi & Bluetooth)
  - Low data rate wireless personal area network (LR-WPAN)
  - Low power consumption
  - Low complexity
  - Low cost
  - Application for biochip

Specification

Features	802.11 b	Bluetooth	ZigBee
Power Profile	Hours	Days	Years
Complexity	Very Complex	Complex	Simple
Nodes/Master	32	7	6400
Modulation	QPSK	FSK, GMSK	BPSK, O-QPSK
Range	100 m	10 m	100 m
Frequency	2.45 GHz	2.45 GHz	2.45 GHz
Data Rate	11 Mbps	1 Mbps	250 kbps
Security	802.1x	64 bit, 128 bit	AES-128bit

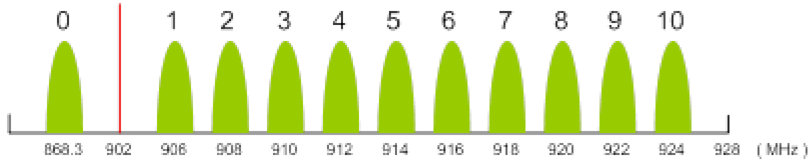
Data rate vs. transmission distance

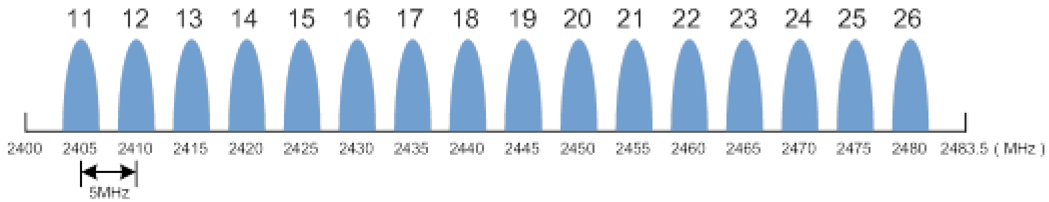


Channel Assignment

PHY (MHz)	Frequency Band (MHz)	Speeding Parameters		Data Parameters	
		Chip Rate (kchip/s)	Modulation	Bit Rate (kb/s)	Symbol Rate (ksymbol/s)
868 / 915	868 - 868.6	300	BPSK	20	20
	902 - 928	600	BPSK	40	40
2450	2405 – 2483.5	2000	O-QPSK	250	62.5

- Europe : 1 channel, 868.3 MHz
- United States : 906~928MHz &10 channels, BW=1.2M, Spacing 2M
- Worldwide : 2400~2483.5MHz &16 channels, BW=2M, Spacing 5M





Receiver Sensitivity Definitions

- The required package error rate (PER) should be less than 1% measured over a random PHY service data unit (PSDU) data.

Term	Definition of term	Conditions
Packet error rate (PER)	Average fraction of transmitted packets that are not detected correctly.	-Average measured over random PSDU data.
Receiver sensitivity	Threshold input signal power that yields a specified PER.	- PSDU length = 20 octets - PER < 1% - Power measured at antenna terminals. - Interference not present.

- The PER is related to the bit error rate (BER) (*IEEE standard 802.15.4-2003*)

$$1\%\ PER = 0.00625\%\ BER$$

Noise Figure and Phase Noise

- With BER = 0.00625%, SNR_{min} = 0.5 dB.
- Sensitivity specification of the 2.4-GHz receiver must be less than -85 dBm.
- The noise figure (NF) of the receiver can be expressed as

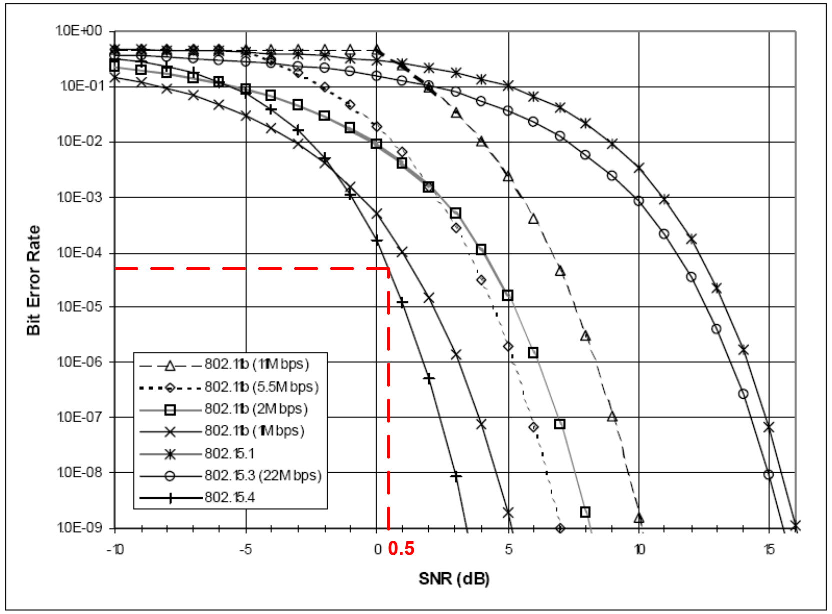
$$NF \le sensitivity - \{-174\,dBm/Hz + 10\log(BW)\} - SNR_{min}$$

- The maximum NF of RF/analog front-end is 20.5 dB.

(Assumed board, external-component,

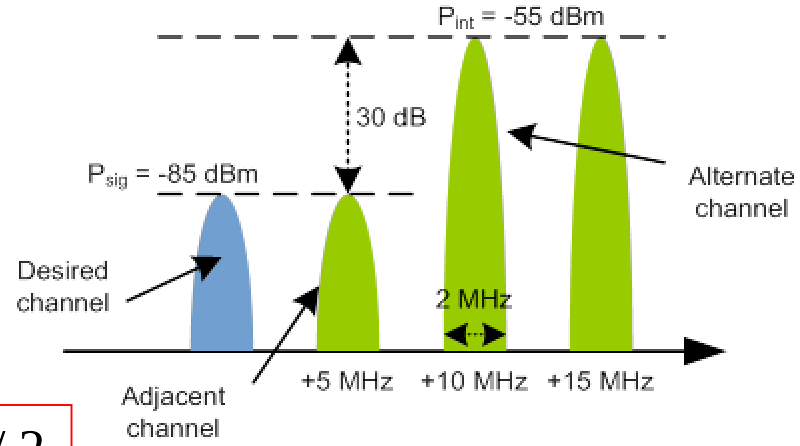
and digital part contributed 5 dB noise figure.)

- The phase noise requirement of the LO is limited by Federal Communication Commission (FCC). The value is about -102 dBc/Hz at 3.5MHz offset.



Receiver Nonlinearity [N. J. Oh, 2006]

- IIP1dB is above -20 dBm with maximum input power -20 dBm.
- IIP3 is above -10 dBm with maximum input power.
- IIP2 is above 10.5 dBm.
- The IIP3 and IIP2 can given by



$$IIP3 = (3P_{int} - P_{sig} + SNR_{min} + Margins) / 2$$

$$IIP2 = 2P_{int} - P_{sig} + SNR_{min} + Margins$$

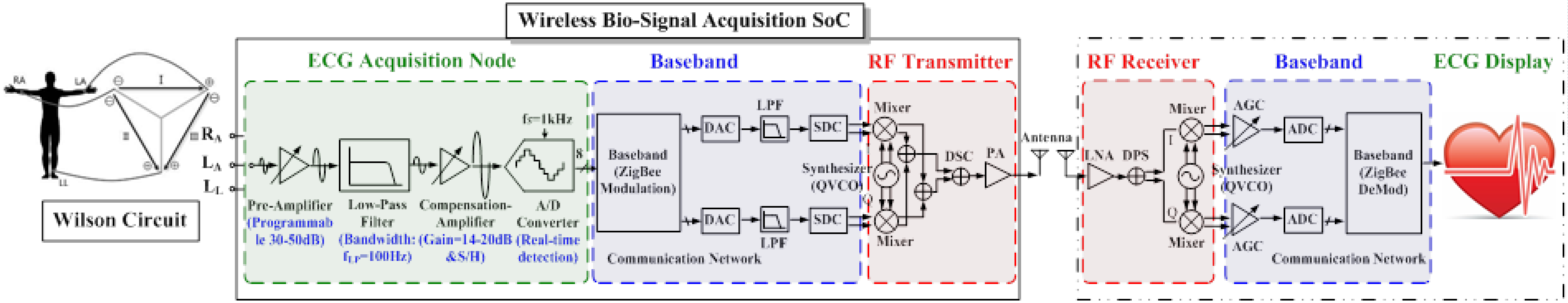
where P_{int} is the power of two interferers (±10 and ±20 MHz apart from the signal), P_{sig} is the power of the desired signal and 10 dB margins.

N. J. Oh, et. al., "Building a 2.4-GHz radio transceiver using IEEE 802.15.4," *IEEE Circuit and Devises Magazine*, 2006.

Receiver Target Specifications

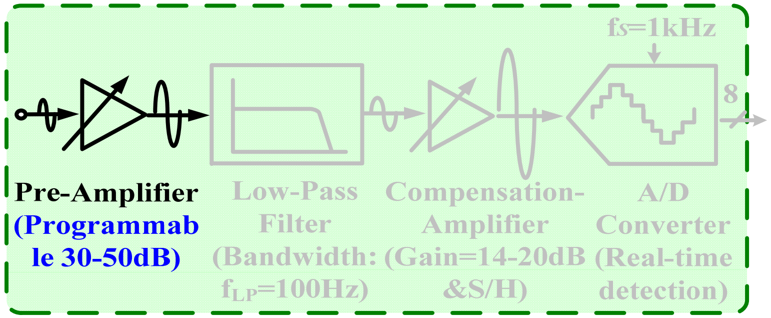
	Items	Specifications
Receiver	Input Power [dBm]	-85 ~ -20 dBm
	Noise Figure [dB]	< 20.5
	P1dB [dBm]	> -20
	IIP3 [dBm]	> -10
	IIP2 [dBm]	> 10.5
LO	Phase Noise [dBc/Hz] @ 3.5MHz offset	< -102

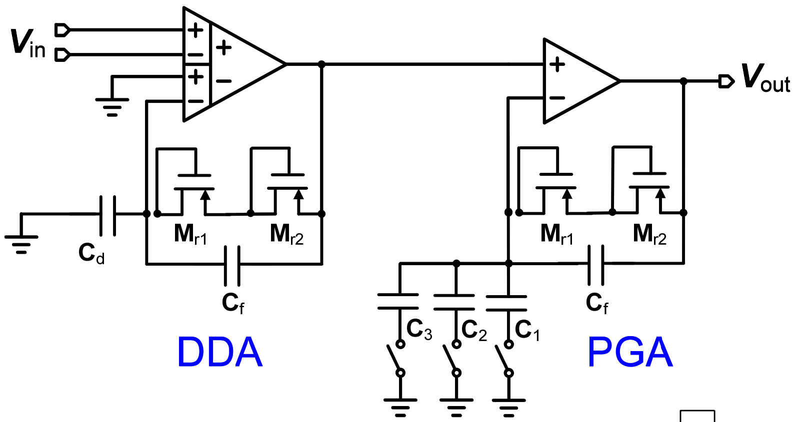
System Block Diagram



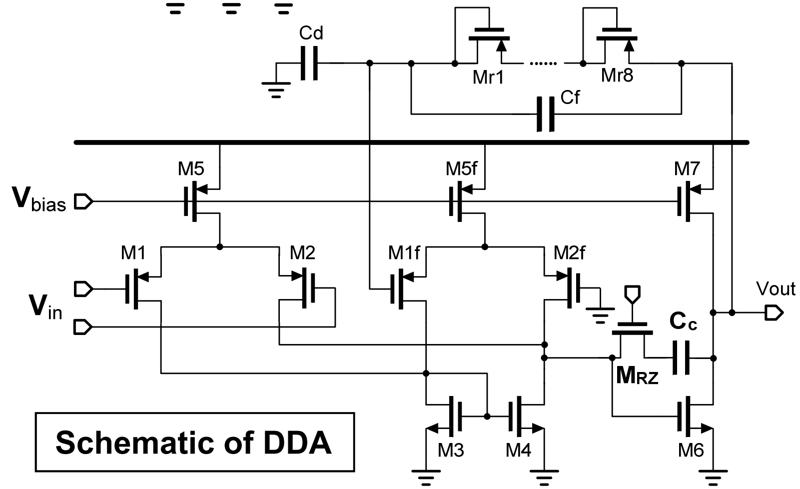
- Transmitter : Wireless Bio-Signal Acquisition SoC (WBSA-SoC)
  - AFE : PreAmp., Filter, PostAmp., 8-bit SAADC
  - Baseband : ZigBee Spread Spectrum Technology
  - Mixed-Mode : DAC, LPF, SDC
  - RF Front-end : VCO, Up-conversion Mixer, PA
- Receiver: ARM Display
  - RF Front-end (ICs) : LNA, DPS, Down-conversion Mixer
  - Mixed-Mode Board: BPF, AGC, ADC
  - Based-Band & Display : ZigBee Demod. & ARM-base Display

ECG Acquisition Node - Preamplifier





- Differential Difference Amplifier(DDA)
  - Pseudo-resistors M_{r1} and M_{r2} ：the provision of DC feedback, decrease the power consumption
  - Capacitors C_d and C_f ：the output gain of DDA
- Programmable Gain Amplifier (PGA)
  - Traditional two-stage operational amplifier
  - Pseudo-resistors M_{r1} and M_{r2} ：the provision of DC feedback, decrease the power consumption
  - Capacitors & switches C_i and C_f ：determination of the adjusted gain ratio

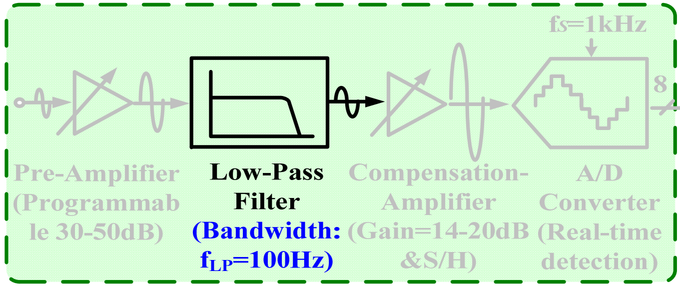


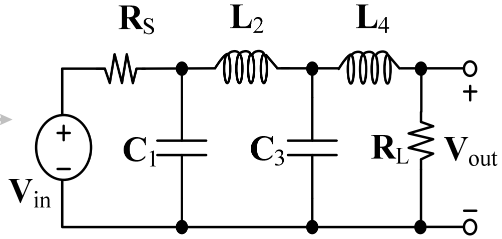
Transfer Function

$$A(s)=\left(1+\frac{sR_fC_d}{sR_fC_f+1}\right)\times\left(1+\frac{sR_fC_i}{sR_fC_f+1}\right)\quad i=1,2,3$$

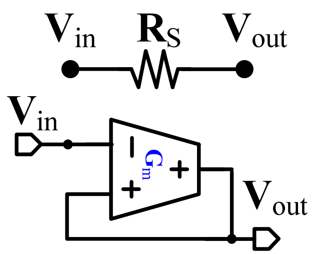
DDA **PGA**

ECG Acquisition Node – LPF [11]

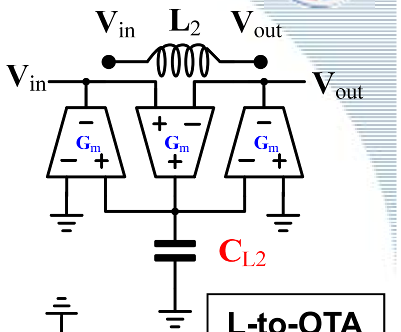




4th ladder type LPF



R-to-OTA



L-to-OTA

- 4^{th} Butterworth LPF with 100Hz cut-off freq.:
  - Ladder RLC LPF -to- OTA-C filter
  - OTA-C instead of R and L
- Operational-transconductance amplifiers (OTA):
  - Current cancellation: (M_{1L}, M_{2L}), (M_{1M}, M_{2M})
    - Reduce current
  - Current division: (M_{11N}, M_{15N})
    - Reduce transconductance
  - Source degeneration resistors: (M_3, M_4)
    - Improve linearity
  - Achieved smaller size and high performance filter

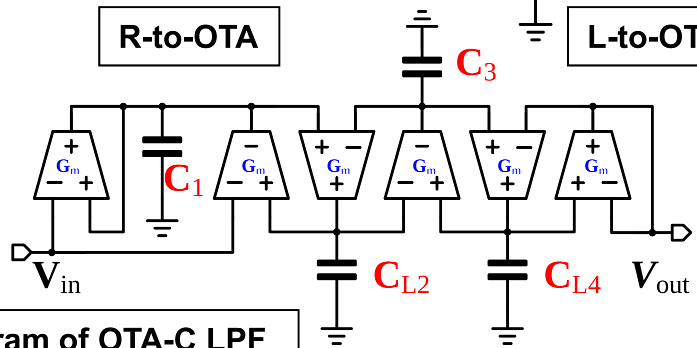
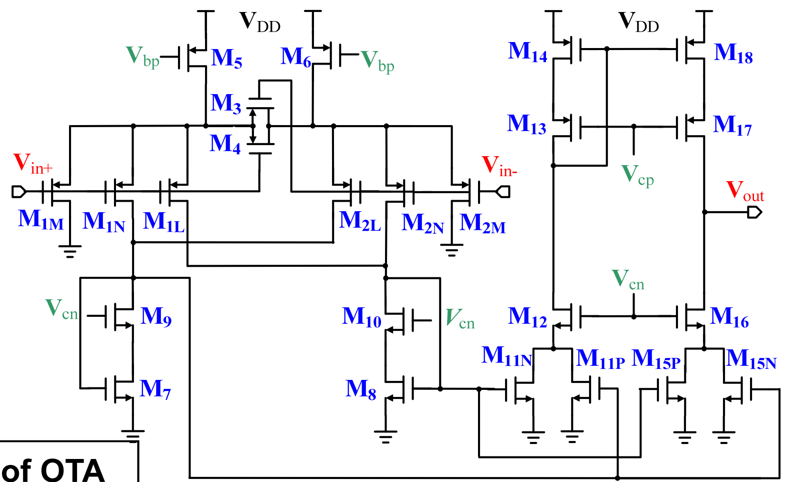


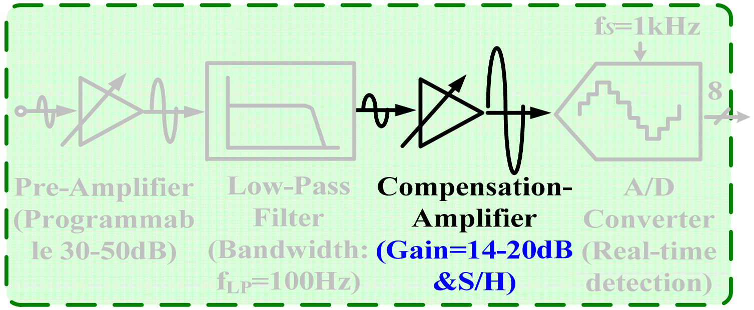
Diagram of OTA-C LPF



[11] S. Y. Lee, et. al." System Design and Modeling of a OTA-C Filter for Portable ECG Detection", *IEEE TBCAS*, Feb. 2008.

Schematic of OTA

ECG Acquisition Node – Post Amplifier



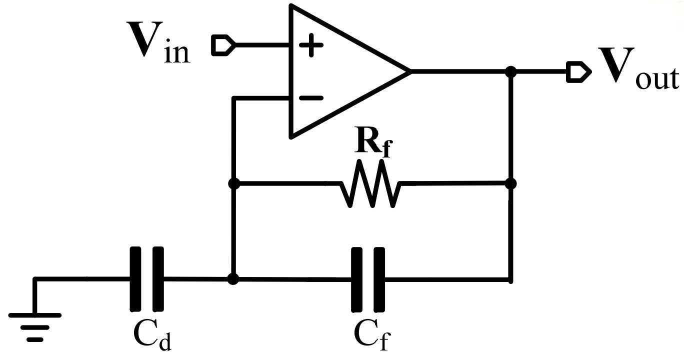
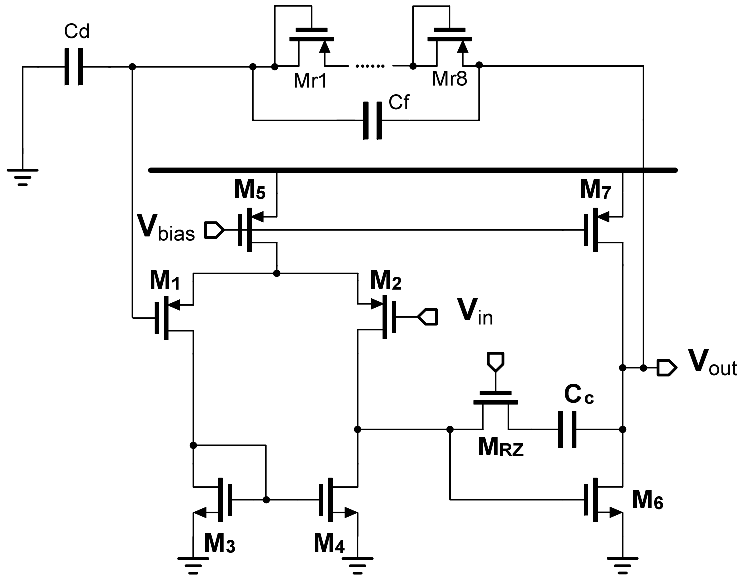


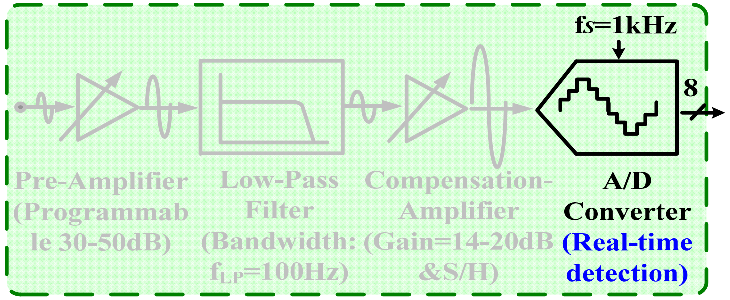
Diagram of Post Amplifier

- Compensation Gain Amplifier
  - Compensate the in-band attenuation of LPF
  - Enhance the voltage amplitude
  - Satisfied the dynamic-range requirement of ADC
- 2nd -stage operation amplifier.
  - Pseudo-resistors R_f ：the provision of DC feedback, decrease the power consumption
  - Capacitors C_d and C_f ：to determine the gain ratio of post amplifier



Schematic of 2nd –stage Amplifier

ECG Acquisition Node – SAADC



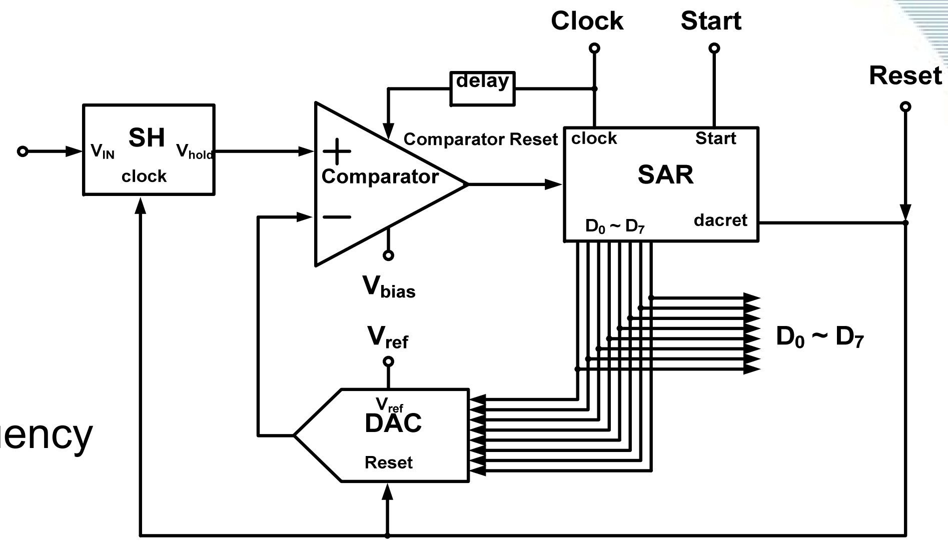


Diagram of SAADC

- Analog/Digital Converter
  - 8-bit SA ADC with 1KHz sample frequency
  - Sample and hold, comparator, DAC, SAR controller
- S/H Amplifier
  - Switch-Capacitive gain circuit for compensation
  - Resettable gain circuit for offset cancellation

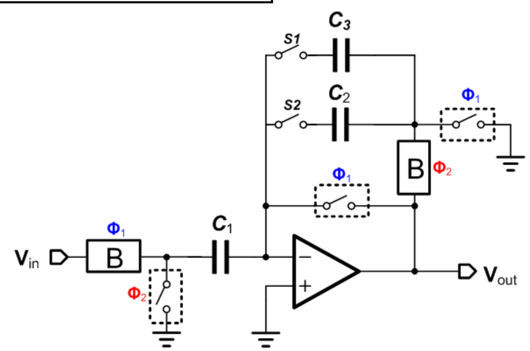
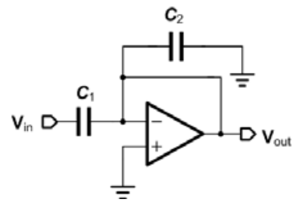
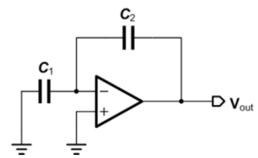


Diagram of S/H



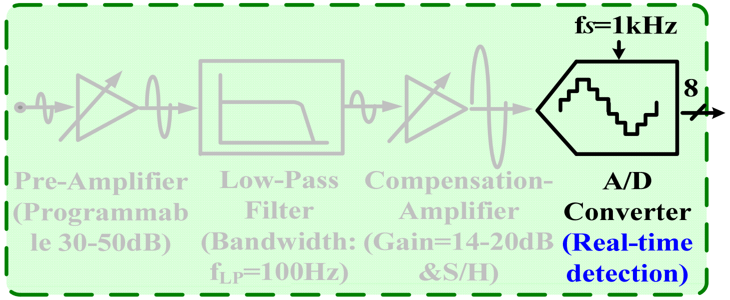
Φ1 : sample mode



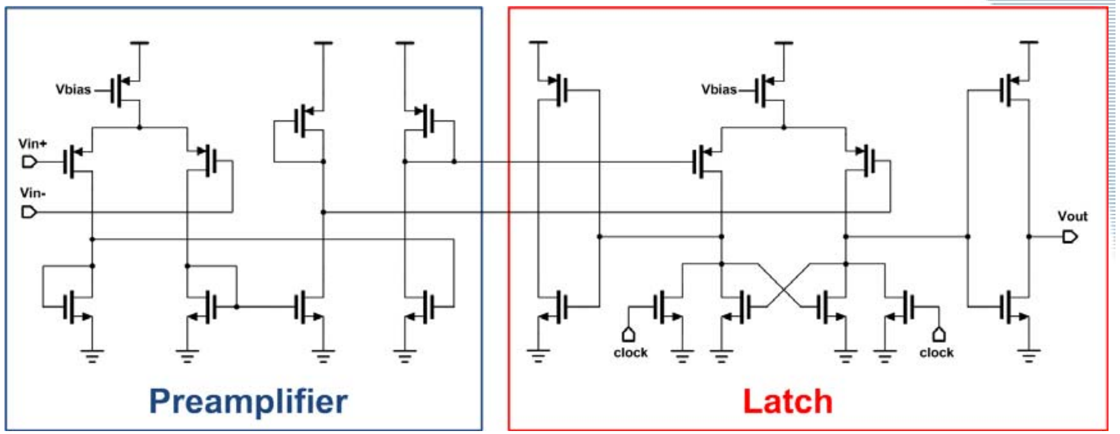
Φ2 : hold mode

B : bootstrap switch

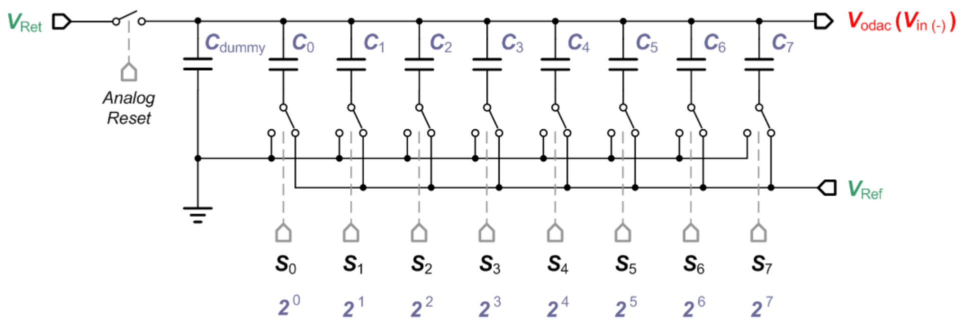
ECG Acquisition Node – SAADC (cont.)



- Comparator
  - Preamplifier stage
    - For obtaining higher resolution
    - Minimizing the effects of kickback noise
  - Positive feedback latch stage
- DAC
  - Charge redistribution D/A Converter



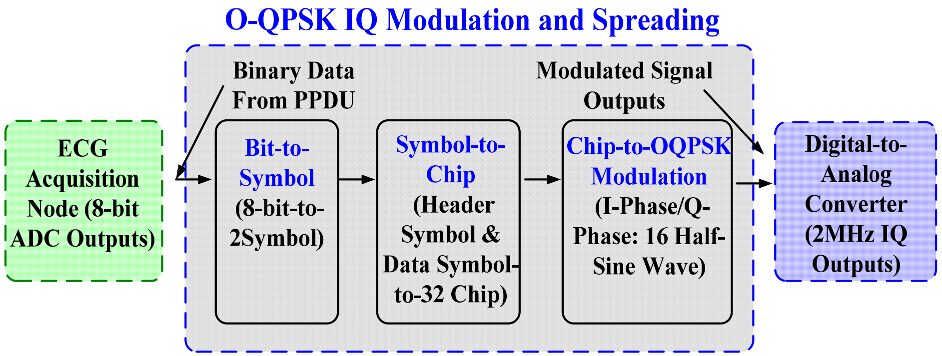
Comparator



DAC

$$V_{odac} = V_{Ret} + V_{Ref}\left(\frac{S_7}{2^1} + \frac{S_6}{2^2} + \frac{S_5}{2^3} + \frac{S_4}{2^4} + \frac{S_3}{2^5} + \frac{S_2}{2^6} + \frac{S_1}{2^7} + \frac{S_0}{2^8}\right)$$

IQ Baseband Communication Network [12]

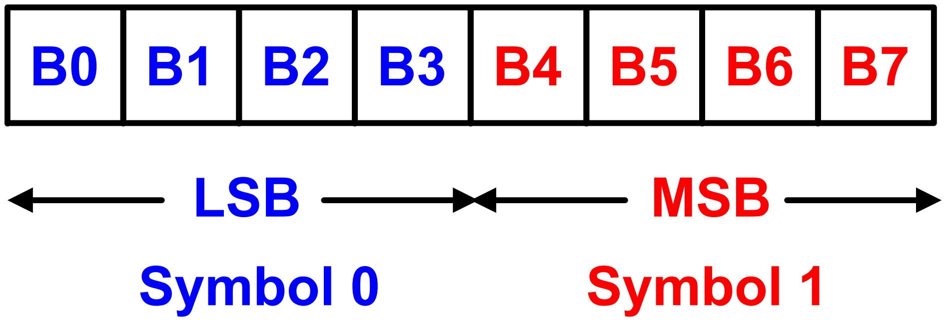


Block diagram of OQPSK modulation

PHY (MHz)	Frequency band (MHz)	Spreading parameters		Data parameters		
		Chip rate (kchip/s)	Modulation	Bit rate (kb/s)	Symbol rate (ksymbol/s)	Symbols
868/915	868–868.6	300	BPSK	20	20	Binary
	902–928	600	BPSK	40	40	Binary
868/915 (optional)	868–868.6	400	ASK	250	12.5	20-bit PSSS
	902–928	1600	ASK	250	50	5-bit PSSS
868/915 (optional)	868–868.6	400	O-QPSK	100	25	16-ary Orthogonal
	902–928	1000	O-QPSK	250	62.5	16-ary Orthogonal
2450	2400–2483.5	2000	O-QPSK	250	62.5	16-ary Orthogonal

ZigBee Specification

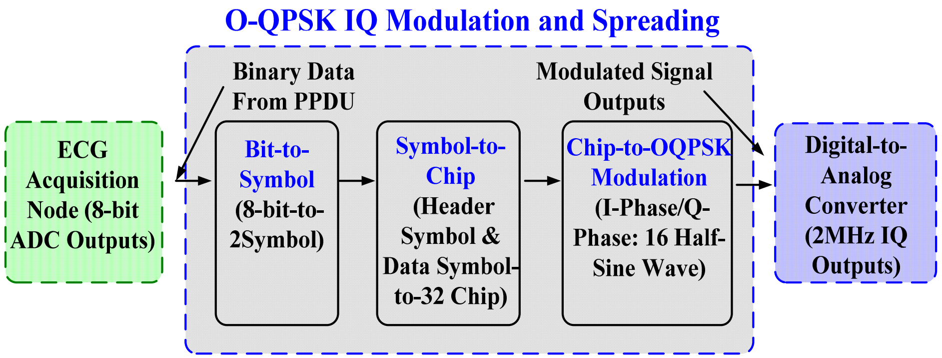
- IEEE 802.15.4 spreading techniques
  - **Bit-to-symbol**
  - **Symbol-to-chips**
  - **Chip-to-OQPSK modulation**
- Bit-to-symbol
  - **8-bit** header and **8-bit** data
  - **8-bit** data -to- **2 symbols**
  - **First Priority**: LSB Symbol (b0,b1,b2,b3)
  - **Second Priority**: MSB Symbol (b4,b5,b6,b7)



Bit-to-symbol

[12] ZigBee Alliance (2007, Oct.). [Online] Available: ttp://www.ZigBee.org.

IQ Baseband Communication Network (cont.)



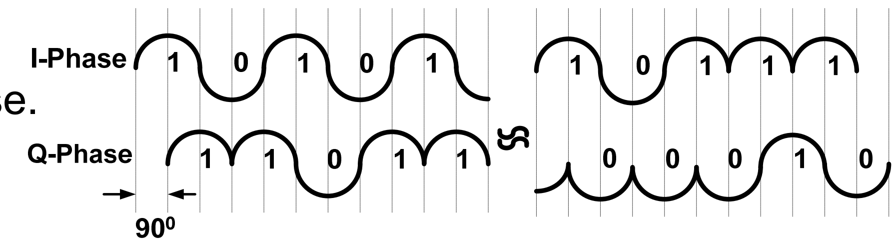
Block diagram of OQPSK modulation

Data Symbol (Decimal)	Data Symbol (Binary) ($b_0\ b_1\ b_2\ b_3$)	Chip Values ($C_0\ C_1 \cdots C_{30}\ C_{31}$)
0	0 0 0 0	1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0
1	1 0 0 0	1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0
2	0 1 0 0	0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0
3	1 1 0 0	0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1
4	0 0 1 0	0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1
5	1 0 1 0	0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0
6	0 1 1 0	1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1
7	1 1 1 0	1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1
8	0 0 0 1	1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1
9	1 0 0 1	1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 1 1 1 1 0 1 1 1 0 1 1 1
10	0 1 0 1	0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 10 1 1 0 0 0 0 0 0 1 1 1
11	1 1 0 1	0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0
12	0 0 1 1	0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0
13	1 0 1 1	0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1
14	0 1 1 1	1 0 0 1 0 1 1 0 0 0 0 0 01 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0
15	1 1 1 1	1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 01 1 1 0 1 1 1 1 0 1 1 1 0 0 0

Mapping table

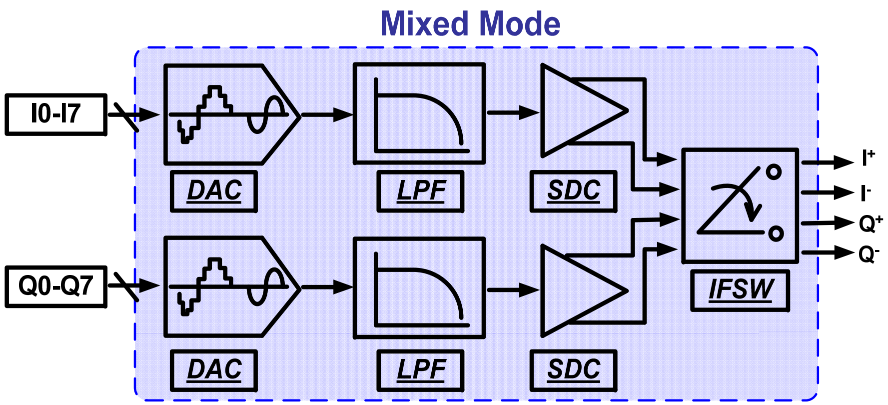
- Symbol-to-32 chips
  - Each data symbol shall be mapped into a 32-chip pseudo-random noise (PN) sequence
  - Mapping table
- Chip-to-OQPSK modulation
  - Q-phase have delayed by 90^0 of the I-phase.

$$p(t)=\begin{cases}\sin\left(\pi\dfrac{t}{T}\right) & ,0\le t\le T\\ 0 & ,\ otherwise\end{cases}$$

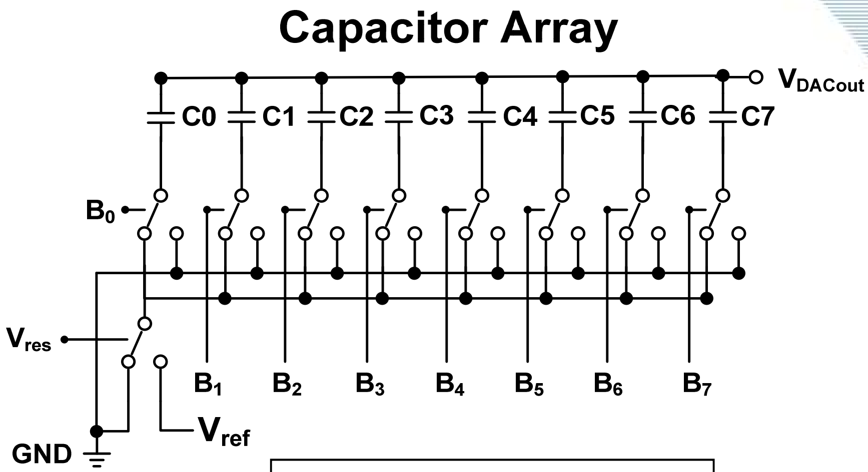


Half-sin pulse shaping

Mixed Mode Circuits

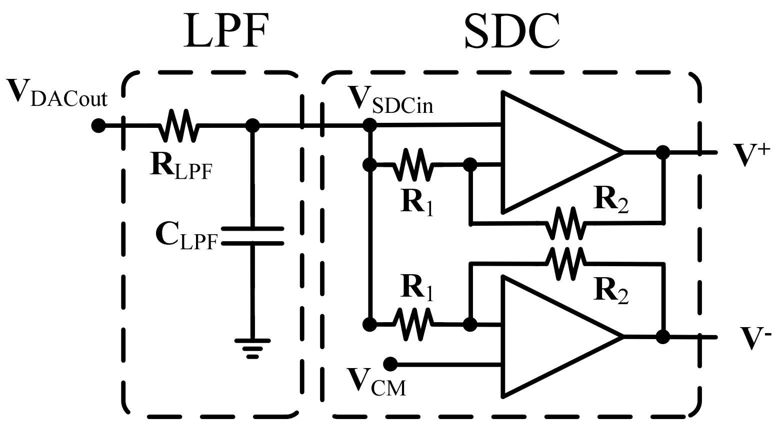


Block diagram of Mixed-Mode circuits



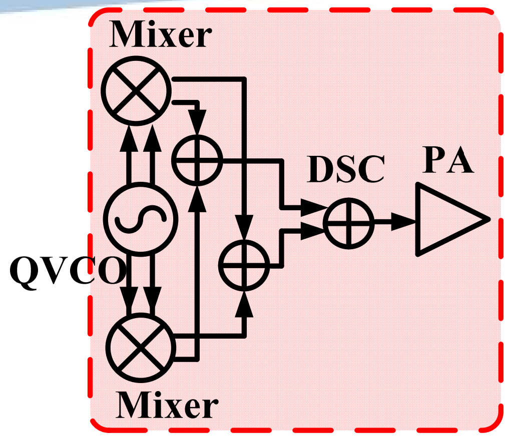
Schematic of DAC circuits

- 8-bit capacitor array DAC
- 1st RC Low Pass Filter (LPF)
- Single-input to differential-out converter (SDC)
  - Line driver system with dual OP
  - With **width bandwidth** and **driving** capability

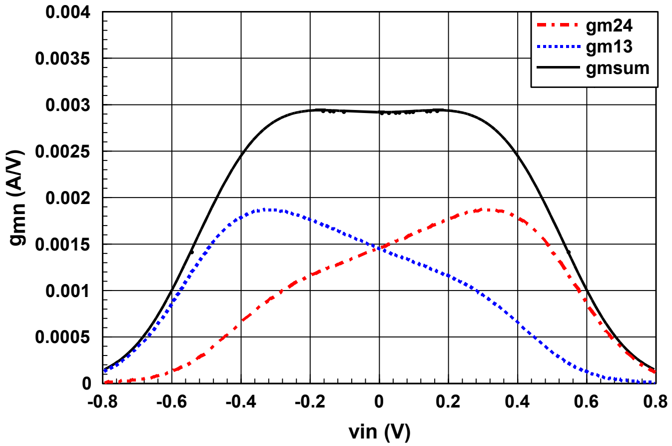


Circuit diagram of LPF and SDC

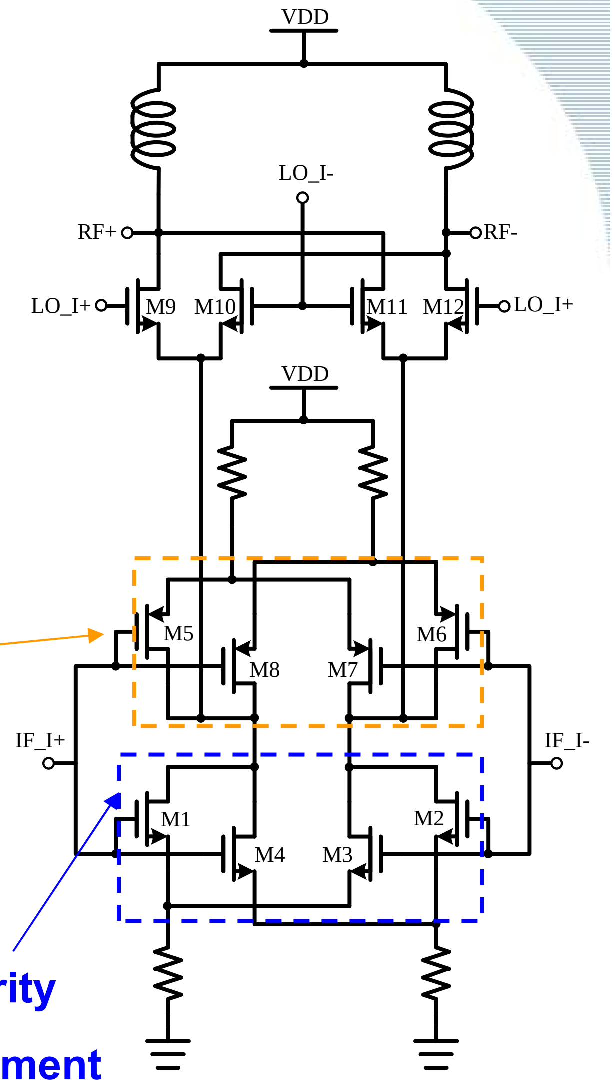
RF Transmitter



Block diagram of RF transmitter



Block diagram of RF transmitter



Schematic of double balance mixer

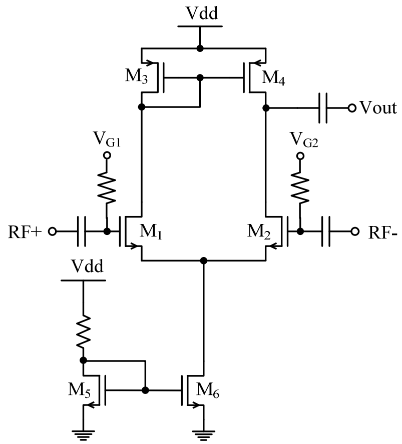
CG Improvement

Linearity Improvement

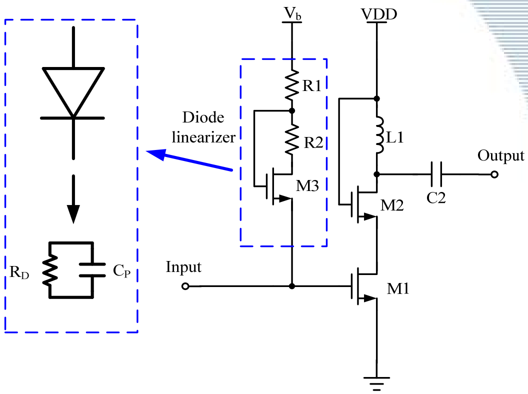
- RF Transmitter:
  - Up-Conversion Mixer, Power Amplifier, QVCO
- Up-Conversion Mixer
  - Double balance structure
  - Linearity improvement by increasing dynamic range
    - Muti-tanh
    - (M_1, M_4) and (M_2, M_3) compensated gm
  - Conversion gain improvement $g_m \Rightarrow (g_{mn} + g_{mp})$
    - Stack PMOS as class AB

RF Transmitter (cont.)

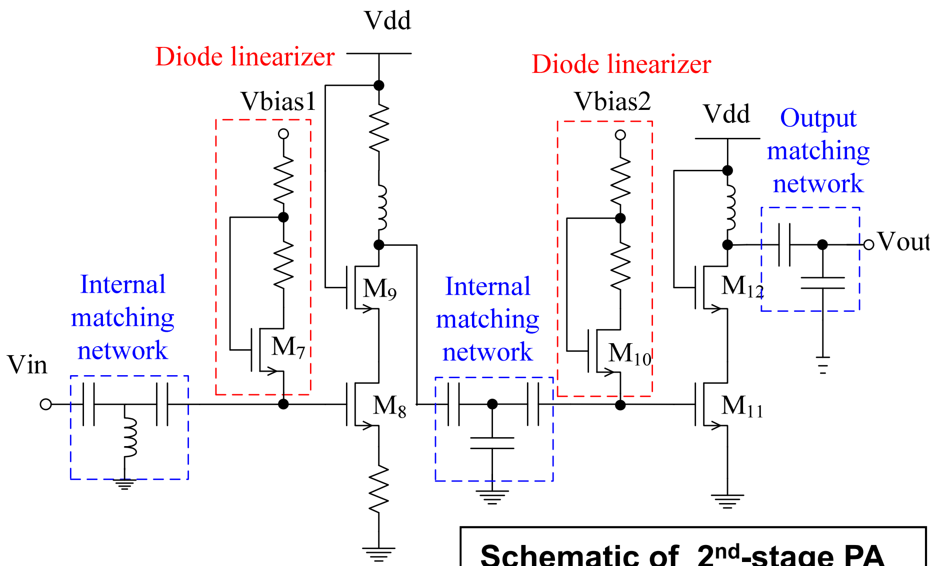
- Differential-to-single converter (DSC)
  - **RF-balun** connected with mixer and PA
  - Differential outputs to single-end input
- 2^{nd}-stage 2.4GHz Power Amplifier
  - **Diode linearizer**
    - Improve linearity
    - Enhance gain compression
    - Share the AC current to avoid saturation
  - **Matching circuits**
    - Internal and output matching network
    - To **attenuate** the conversion gain out of 2.4GHz band
    - To obtain the lower **insertion loss**



Schematic of DSC



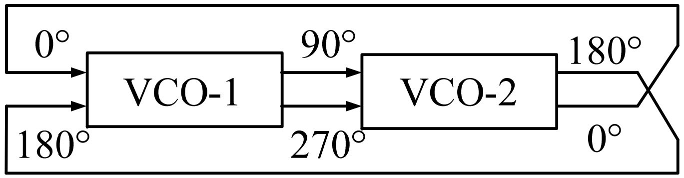
Schematic of diode linearizer

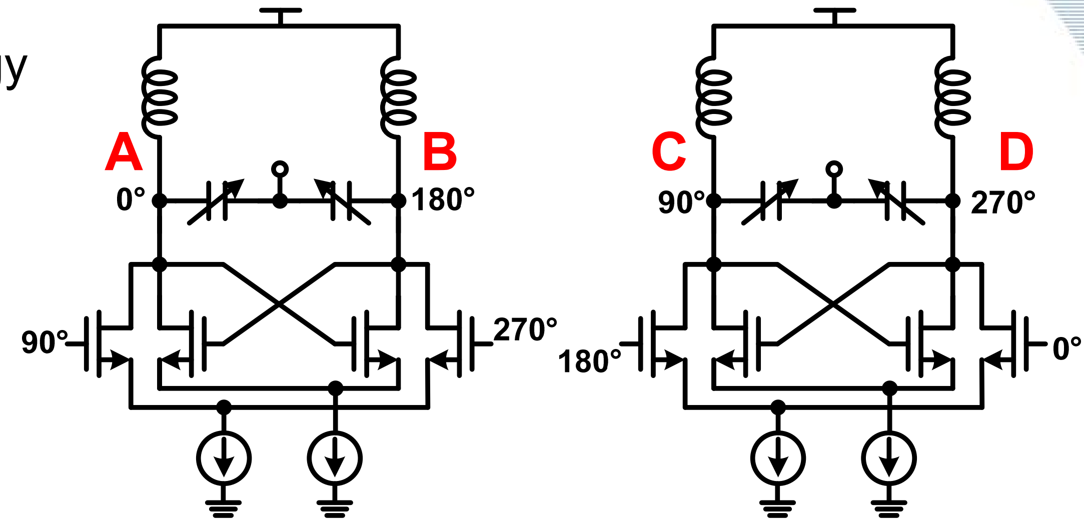


Schematic of 2nd-stage PA

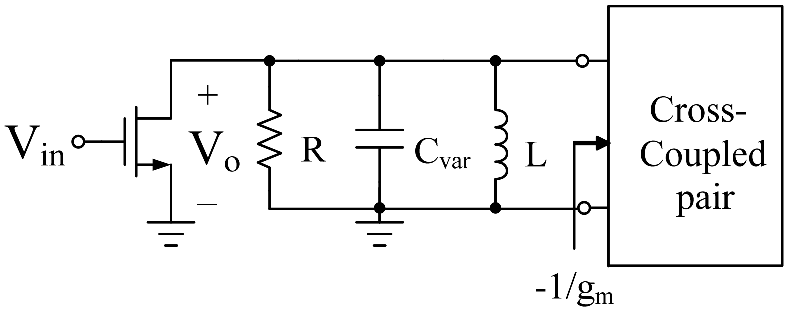
Quadrature VCO

- Conventional QVCO topology





- 90 degree shift analysis



$$\frac{V_o(s)}{V_{in}(s)} = \frac{-g_m LRS}{S^2 LCR + SL + R}$$

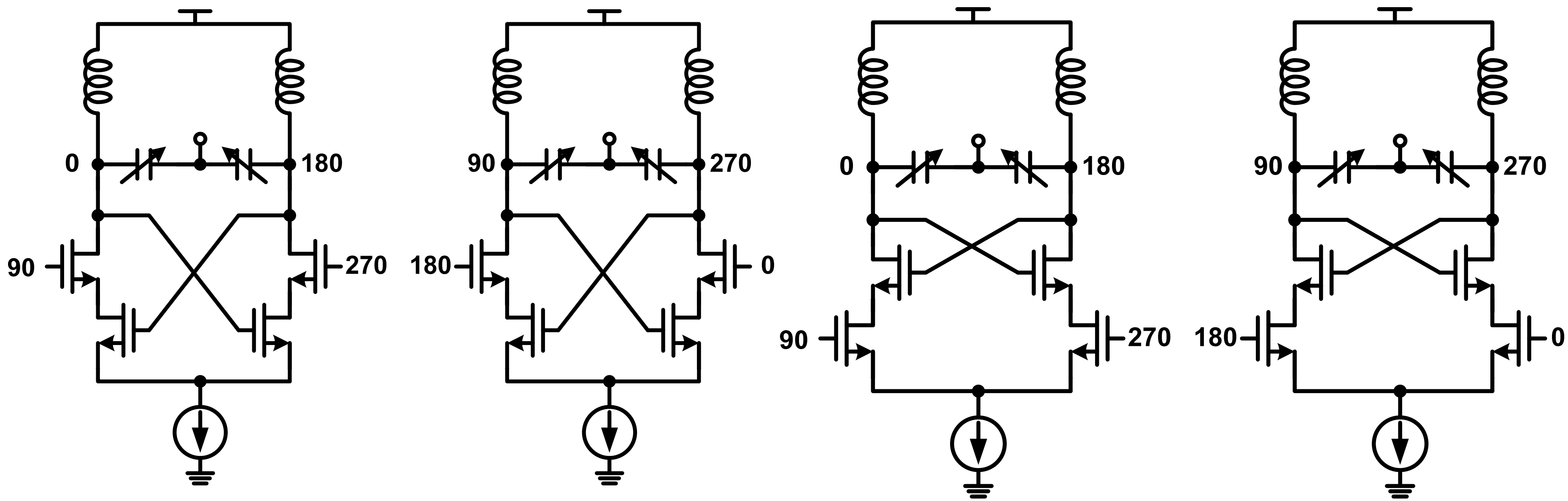
$$(R // \frac{-1}{g_m} \to \infty)$$

$$\frac{V_o(s)}{V_{in}(s)} = \frac{-g_m LS}{S^2 LC + 1}$$

- Drawbacks
  - **High power** : 8-current paths.
  - **Narrow tuning range** : large parasitic capacitors that reduce the tuning range.

Improvements of QVCO

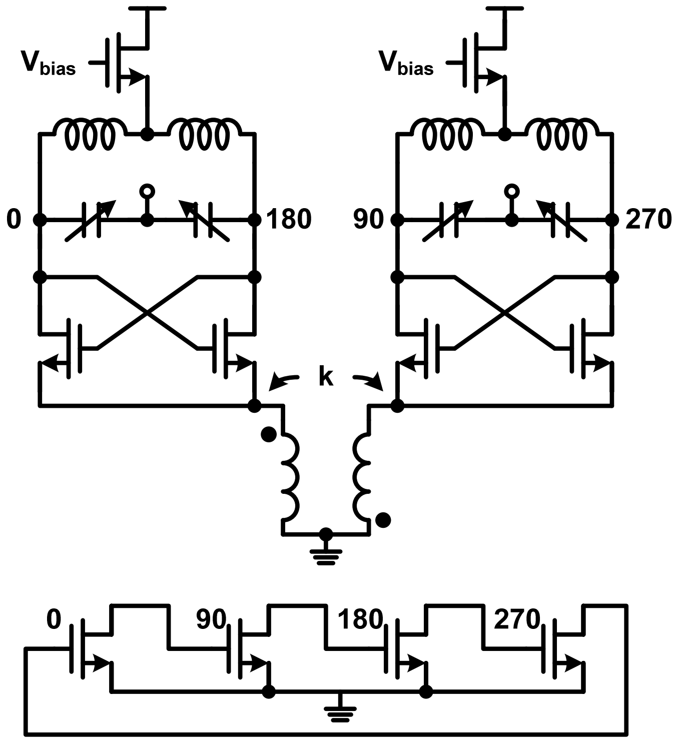
- Top series [13]
  - **Enhanced tuning range** : reduce parasitic capacitors.
  - **Better phase accuracy**
  - **Worse phase noise**
- Bottom series [14]
  - **Enhanced tuning range** : reduce parasitic capacitors.
  - **Worse phase accuracy**
  - **Better phase noise**



[13] P. Andreani, et. al."Analysis and design of a 1.8-GHz CMOS LC quadrature VCO," *IEEE J. Solid-State Circuits*, Dec. 2002..
[14] P. Andreani, "A 2GHz, 17% tuning range quadrature CMOS VCO with high figure-of-merit and 0.6° phase error," ESSCC, 2002

Improvements of QVCO (conts)

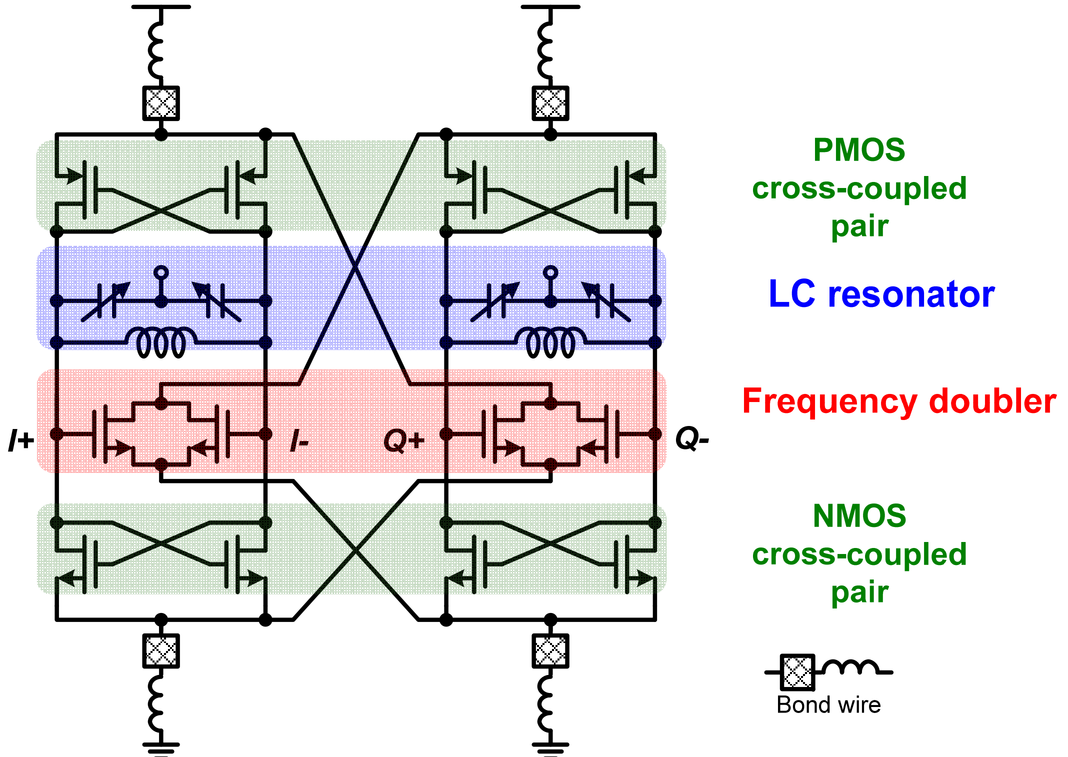
- Common mode inductive coupling [15]
  - Advantages
    - **Enhanced tuning range** : reduce parasitic capacitors.
    - **Low phase noise** : coupling network non-increase phase noise.
- **Disadvantage**
  - **Large chip size** : transformer feedback coupling.



[15] S. L. J. Gierkink, et. al, "A low-phase-noise 5GHz quadature CMOS VCO using common-mode inductive coupling," ESSCC 2002.

Sub-harmonic Injection-Locked Quadrature VCO

- **Advantages**
  - **Low power** : require 4-current paths only
  - **High linearity** : Complementary cross-coupled pair push-pull operation enhanced gain to improve the circuit linearity ⇒ phase noise
  - **Low phase noise** : reduce parasitic resistance to decrease phase noise
  - **Small chip size** : without transformer.



Operation of SHIL-QVCO [16]

- Phase: Quadrature Outputs

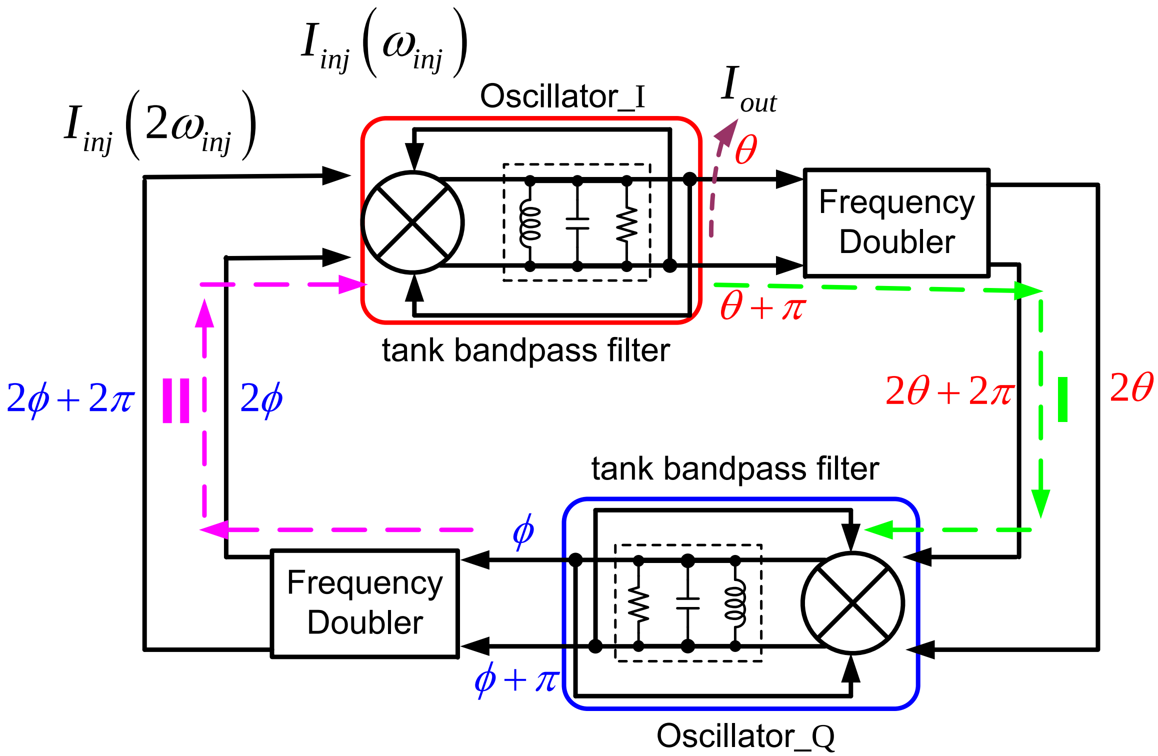
$$(2\theta + 2\pi) - (\phi + \pi) = \phi$$

$$\Rightarrow (\phi - \theta) = \frac{\pi}{2}$$

- Frequency: Injection-locked
  - Mixer + tank bandpass filter

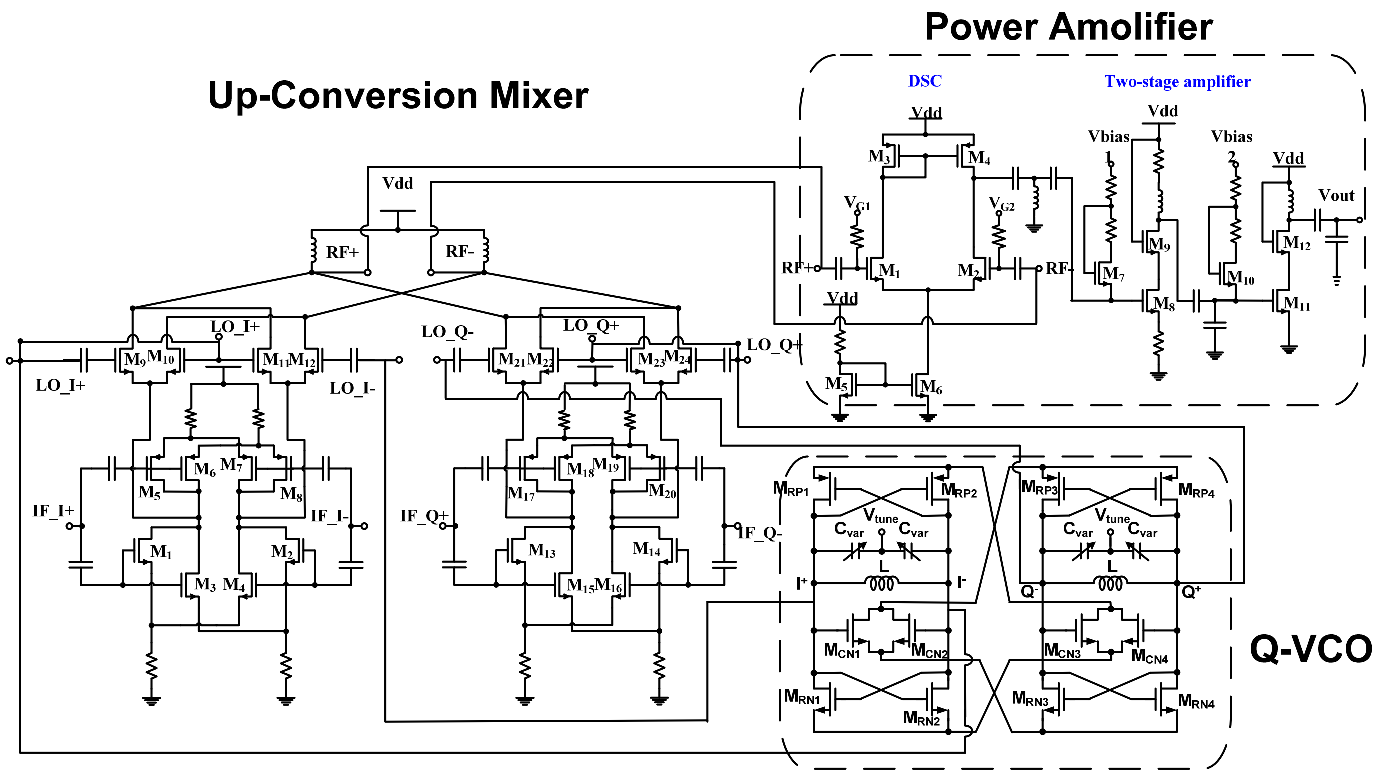
$$I_{inj}(\omega_{osc}) + I_{inj}(3\omega_{osc})$$

- Sub-Harmonic Injection-Locked Quadrature VCO



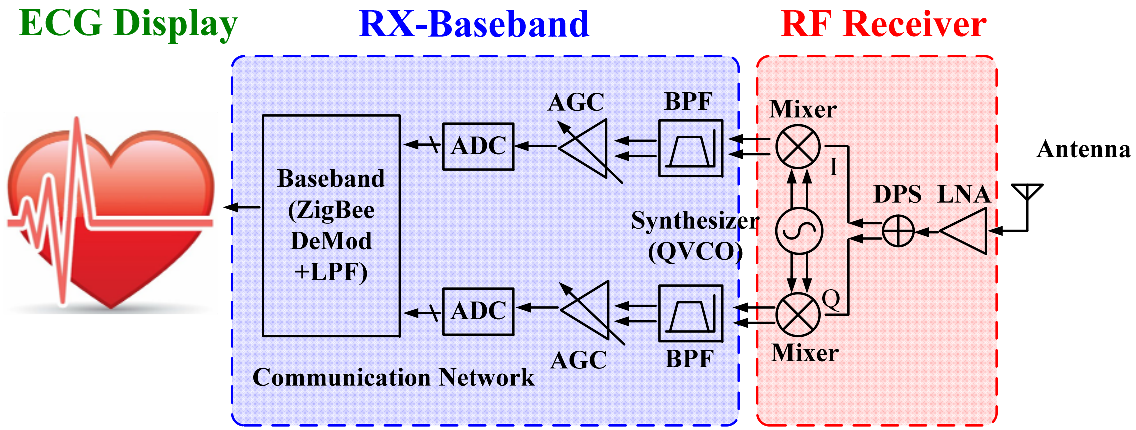
[16] S. Y. Lee, et. al., "A CMOS quadrature VCO with subharmonic and injection-locked techniques," *IEEE TCAS II, 2010.*

RF Transmitter (cont.)



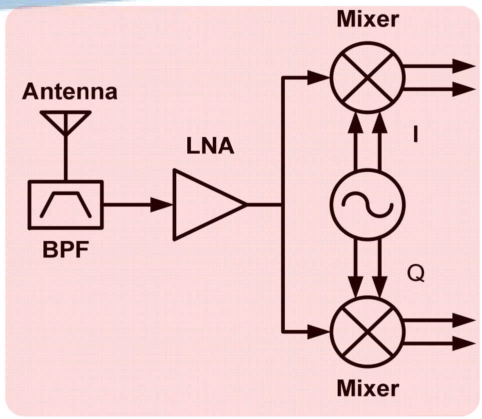
- RF transmitter
  - Mixer: multi-tanh and stacked PMOS to improve the linearity and the conversion gain
  - PA: diode linearizer to improve the gain compression, linearity, and to avoid saturation
  - Quadrature-VCO: sub-harmonic and injection-locked techniques to obtain the quadrature output and to reduce the chip area.

Receiver Block Diagram

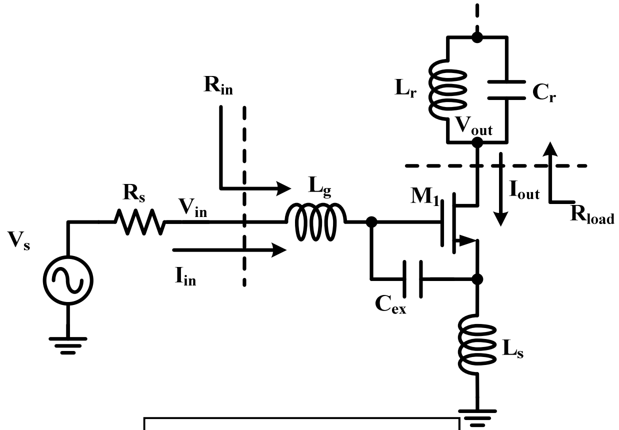


- Receiver: ARM-based Display
  - RF Front-end : LNA, DPS, Down-conversion mixer
  - Mixed-Mode Board: BPF, AGC, ADC
  - Based-Band & Display : ZigBee Demod. & ARM-base Display

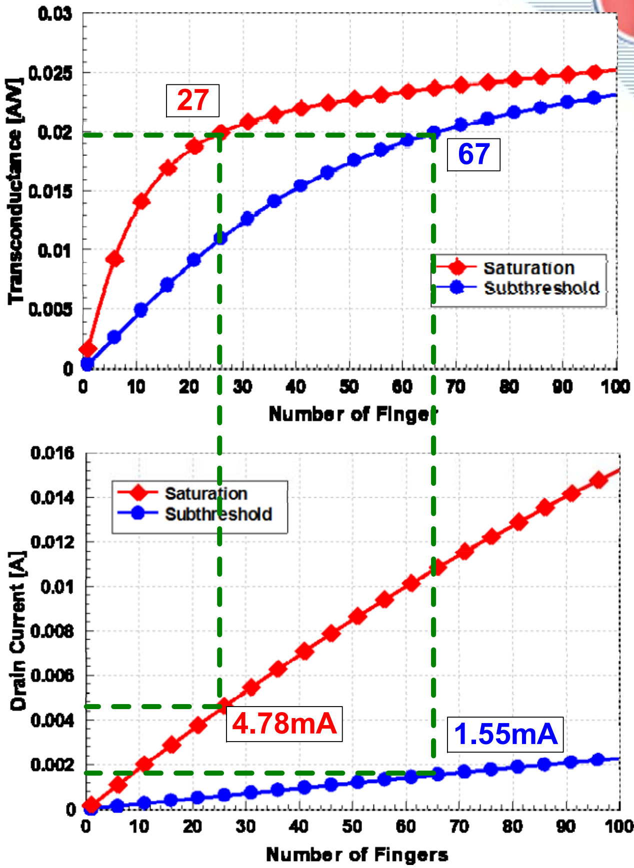
RF Receiver



Block diagram of RF Receiver



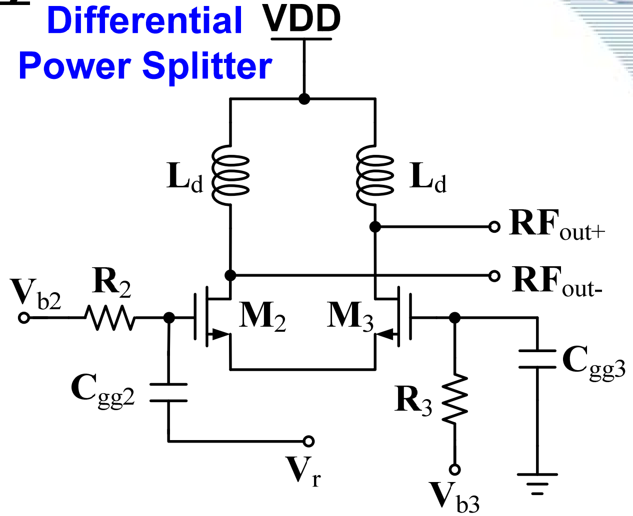
Schematic of LNA



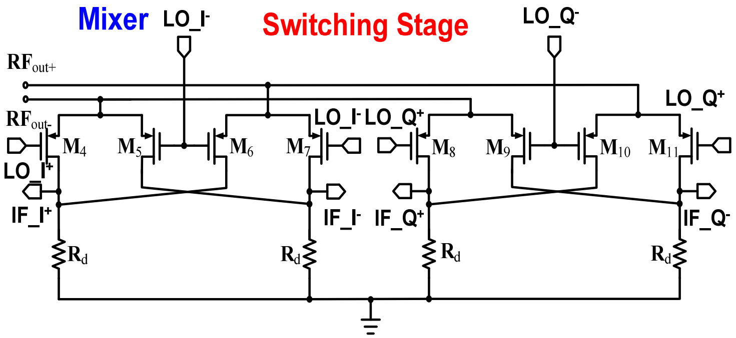
- RF Receiver:
  - LNA, Down-Conversion Mixer, DPS
- Low noise amplifier
  - **High power gain** and **low noise figure**
  - **M_1** CS amplifier with inductive **L_s** source degeneration (optimum noise matching)
  - (g_m/I_{DS}) in the sub-threshold region larger > saturation region
  - **L_r and C_r** can provide high impedance to isolate the RF signal.
  - **R_{load}** is the real part of resonating impedance, **R_{out}** is the output resistance of M_1.

RF Receiver (cont.)

- **Differential Power Splitter**
  - Single-end input to differential out
  - Between LNA and down-conversion mixer
  - M_2 and M_3 are CS and CG amplifier
  - Enhance the conversion gain.
  - DPS stacked on the LNA to reuse the current
- **Quadrature Down-Conversion Mixer**
  - The **thermal noise** can be suppressed by high gain LNA and DPS
  - The flicker noise of **PMOS < NMOS**.
  - **PMOS** is selected to be LO **switching stage**.
  - A **folded-cascode**, **current reused** mixer:
    - Sufficient voltage gain
    - Diminish the thermal noise

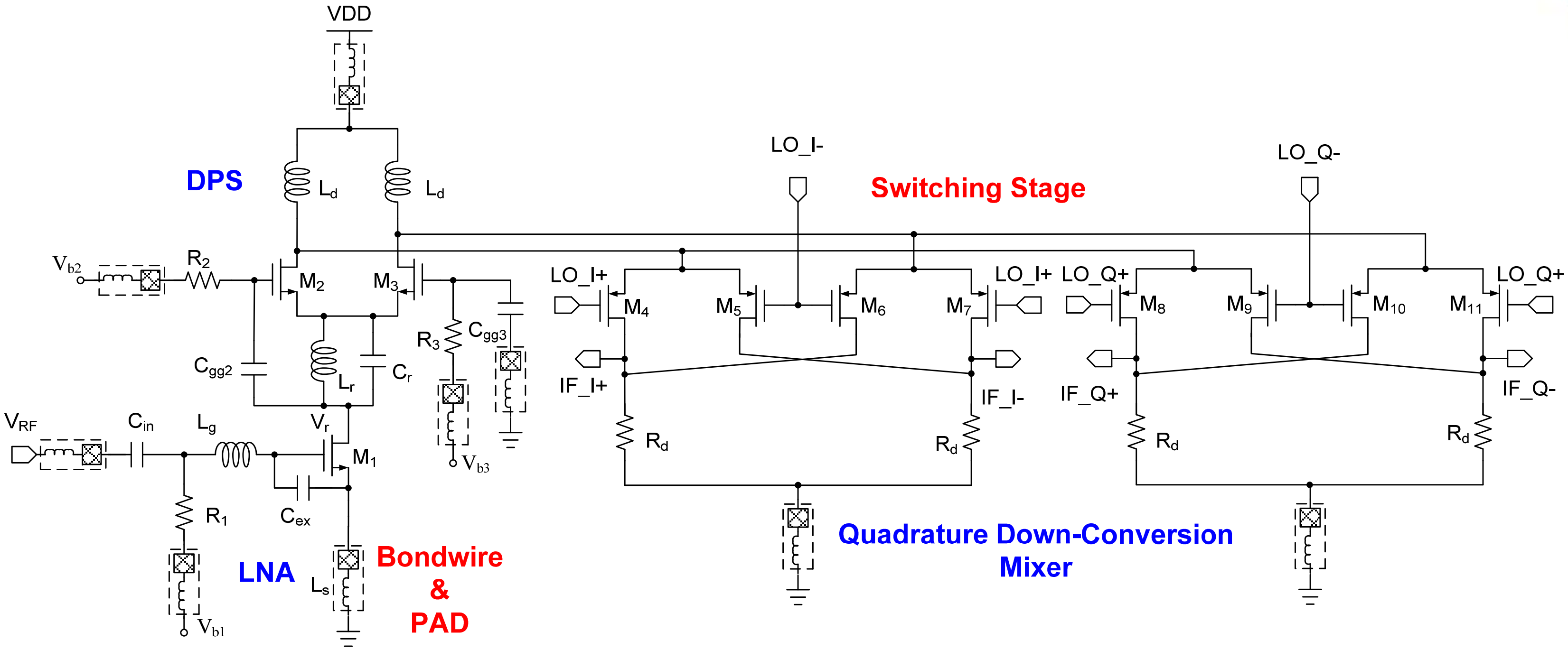


Schematic of DPS



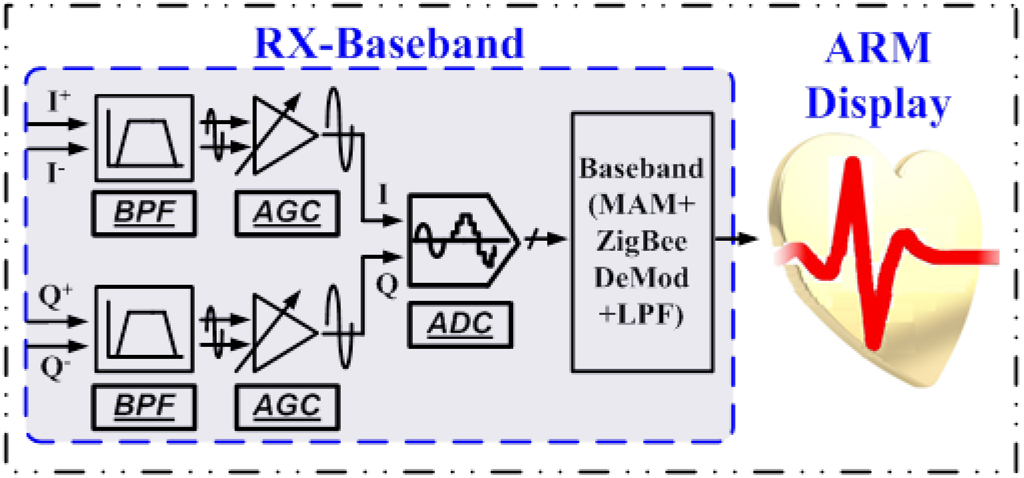
Schematic of Mixer

RF Receiver (cont.)



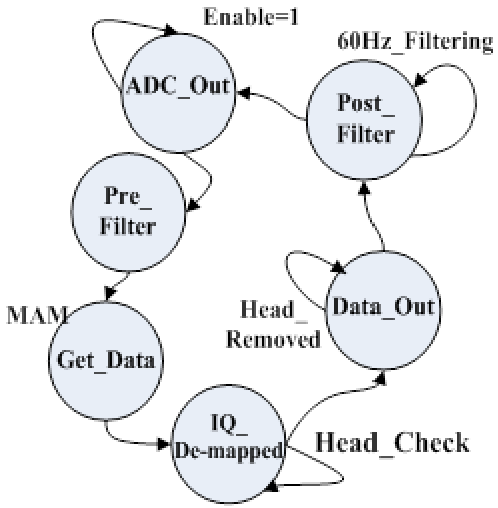
- RF receiver
  - **Low power consumption** : **Current-reused** configuration and **subthreshold** biasing.
  - **High gain** : consist of two gain stages.
  - **Low supply voltage** : folded-cascode mixer configuration
  - **Low noise figure**: suppressed with high gain and low bias current of LO stage.

Mixed Mode Circuits

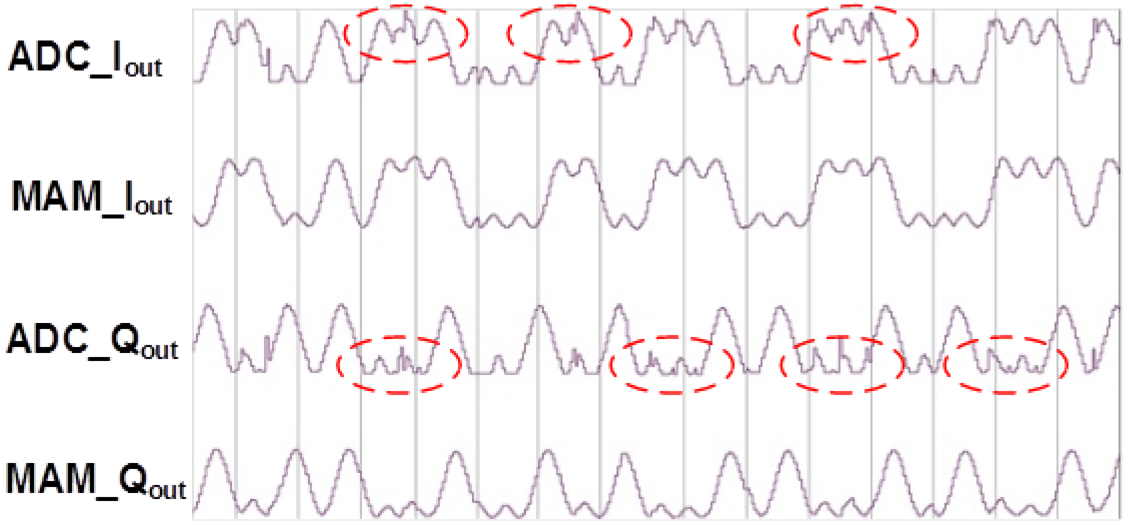


- Analog-to-Digital Mixed-Mode Board
  - Interface: RF front-end receiver - digital baseband processor
  - BPF**: 2nd HPF** with BW of **30 kHz** and **1st LPF** with BW **of 280 KHz**.
  - AGC: amplify quadrature baseband signal, **convert the differential input to single-end output**.
    - **The INA217**, lower DC supply voltage, wide operation BW.
  - ADC**: AD9201** with **dual channel** and **10-bit resolution**
    - Rising edge, falling edge of the clock, to convert I-phase and Q-phase signals.

Offset-QPSK Demodulation



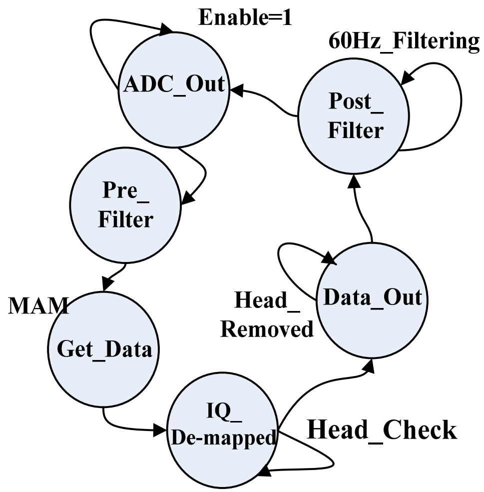
Procedure of Demod



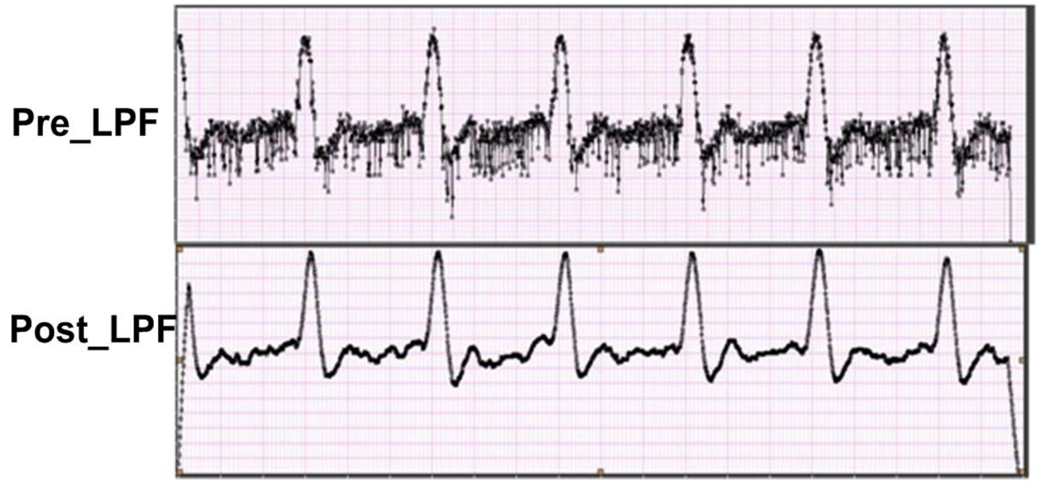
Data out of ADC vs. MAM

- Offset-QPSK Demodulation
  - Input: dual 10-bit I/Q channel digitization codes.
  - Pre_filter:
    - Digitization data with noise interference converted from ADC.
    - **Moving average method (MAM):**
      - Modify the waveform-distribution
      - Enhance the data identification.

Offset-QPSK Demodulation (cont.)



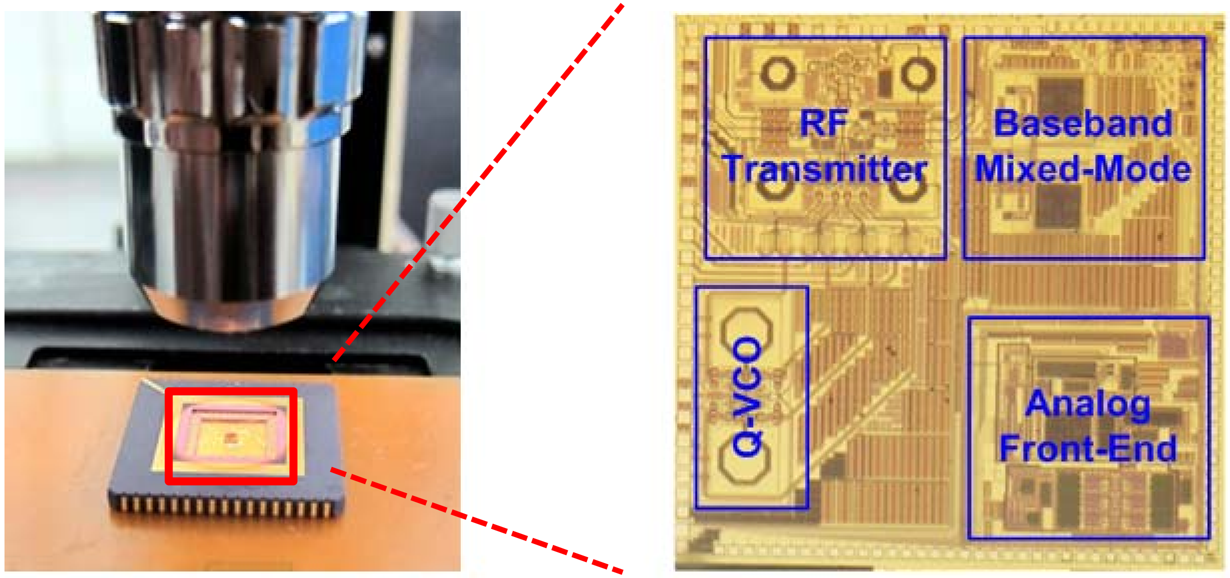
Procedure of Demod



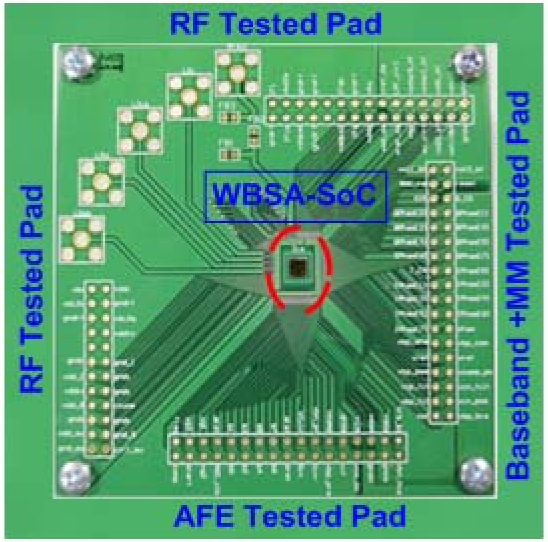
ECG output of Pre_LPF vs. Post_LPF

- Get_data: data stored in shift registers embedded in the FPGA
- IQ De-mapped: leading header and the ECG examination data
- Data_out and Post_filter:
  - Data is stored in shift register
  - **60-Hz instrument noise** interference
  - **256-order** FIR LPF
  - ARM-based displayer with FPGA will display the ECG waveform

Microphotograph, Verification Board



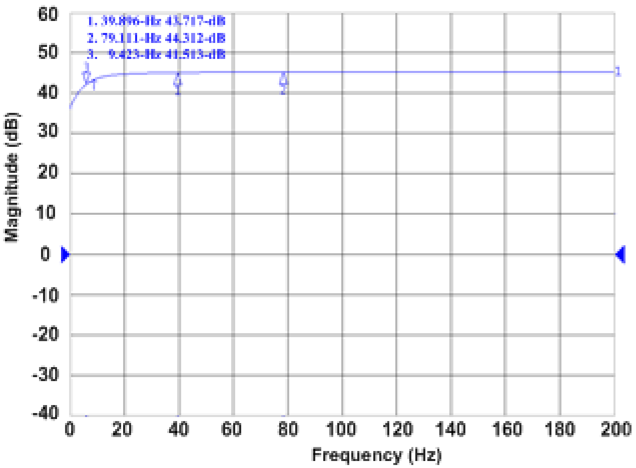
Chip Microphotograph



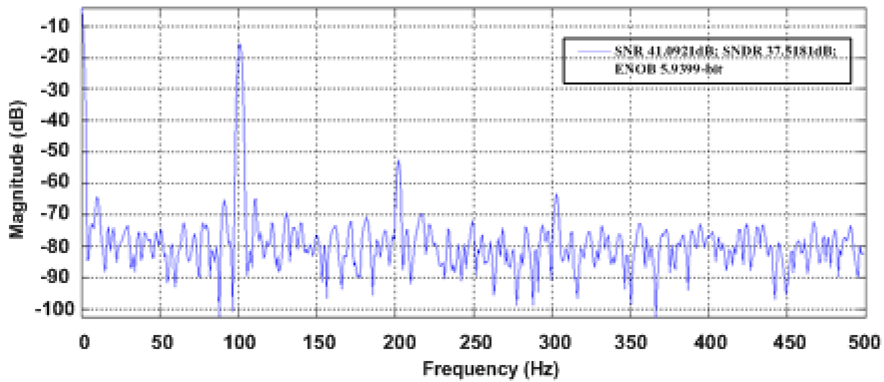
Chip Testing Board

- WBSA-SoC
  - TSMC 1P6M CMOS Process
  - Size = 3mm×3mm
  - Hollowed wire-bond onto PCB with gilding
  - Bondwire line is 3mm

Analog Front-End Measurement Result



Preamplifier Transfer Function

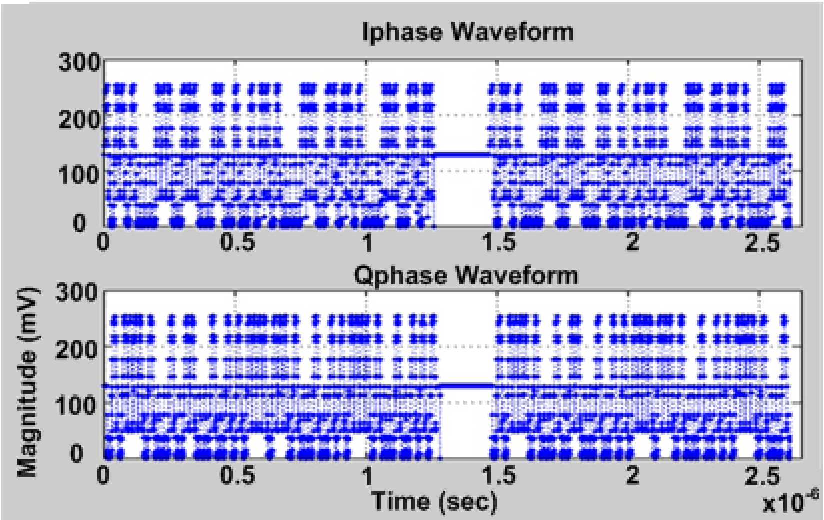


SAADC Measured Spectrum

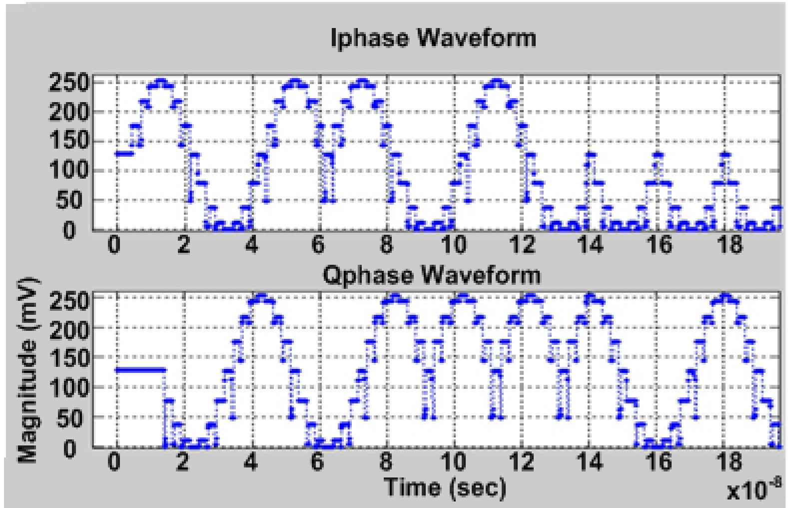
$$ENOB = \frac{SNDR - 1.76}{6.02}$$

- Preamplifier:
  - **SR785** dynamic signal analyzer
  - The **3dB** bandwidth is approximately at **10 Hz**, and the maximum gain of **44.3 dB**,
  - ECG signal of **100 μV to 4 mV** could be amplified to be **15.8mV to 634 mV**.
- SAADC
  - Input signal : **1V$_{pp}$** input swing at **100 Hz** and **1 kHz** sampling rate.
  - SNR: 41.1dB, SNDR: 37.52dB, ENOB : **5.94 bits**

Baseband Measurement Result



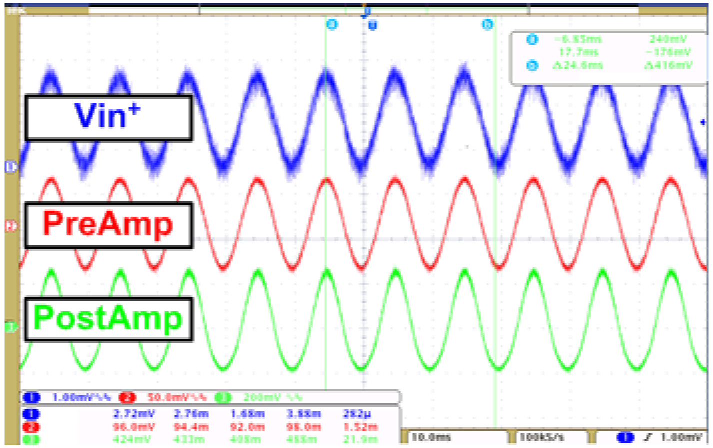
I/Q Modulation



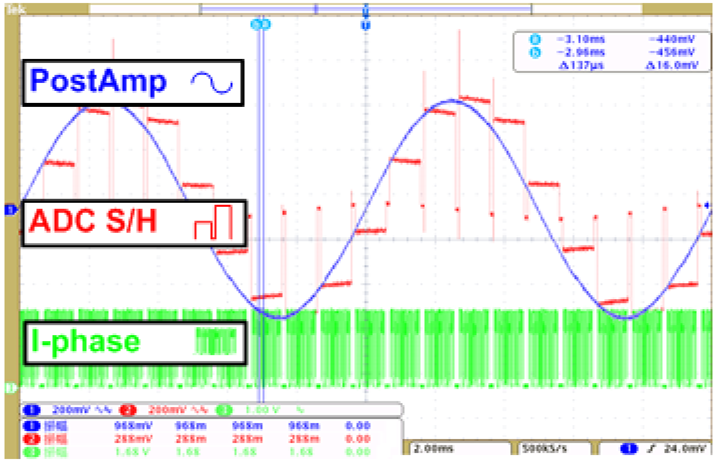
90^0 offset between I-phase and Q-phase

- I-phase, Q-phase Digital Modulation
  - Agilent 16901A logic analyzer and Matlab simulator
  - Half-sine pulse shaping of **I-phase and Q-phase** dual channels
  - **Phase difference** between dual channels (I-phase leading Q-phase 90^0)

AFE, Baseband, Mixed-Mode Measurement Result



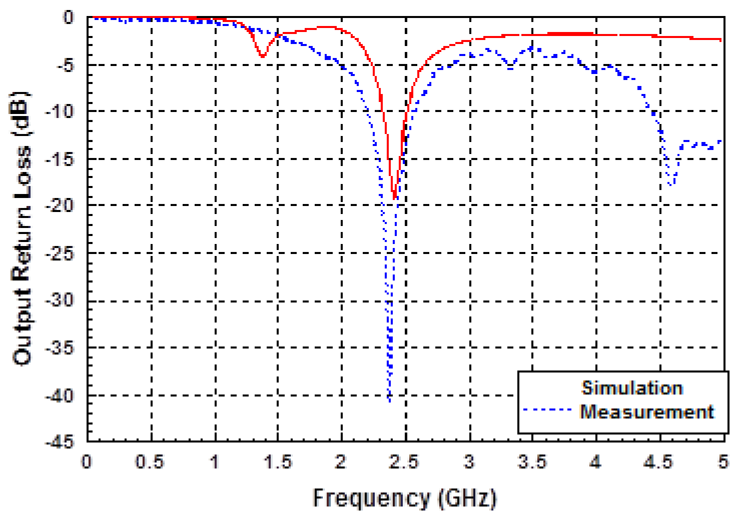
Output swing of Vin, PGA, Post-Amp



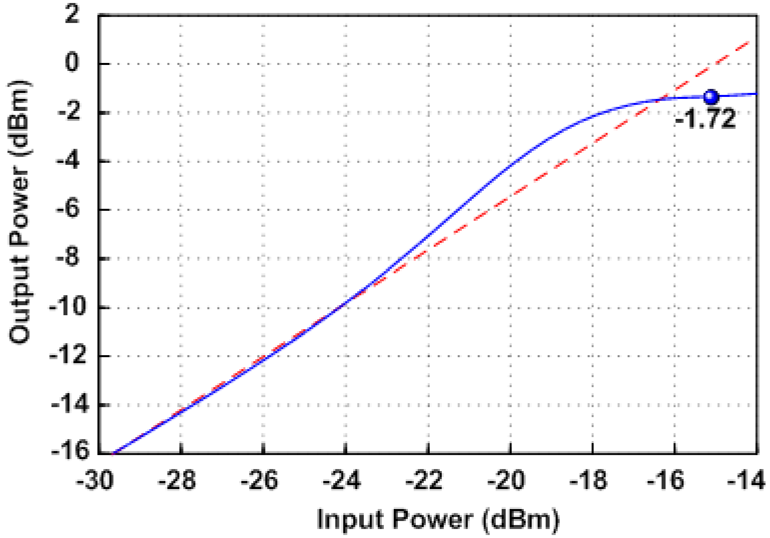
Post-Amp ,ADC S/H, and I-phase

- AFE:
  - Input signal **: 2 mV$_{pp}$** input swing at **100 Hz**
  - Preamplifier and post amplifier outputs are **96 mV** and **420 mV**
  - The conversion gains of PGA and post amplifier are **33 dB** and **52 dB**.
- Mixed-Mode:
  - I-phase modulation signal converted from I/Q baseband to an analog signal.
  - IF signal

RF Transmitter Measurement Result



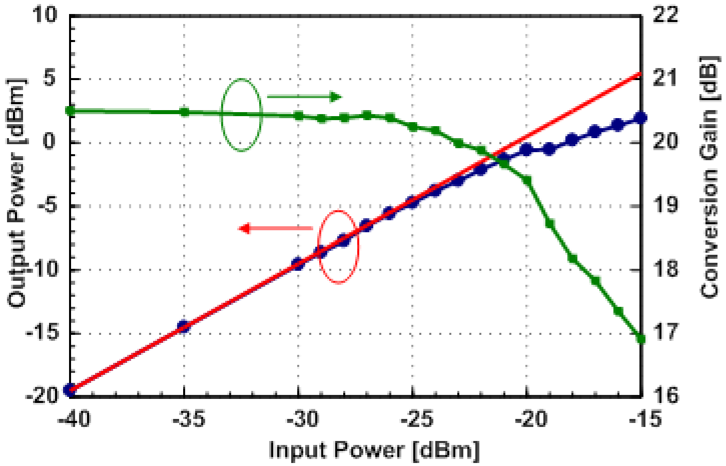
Output Return Loss



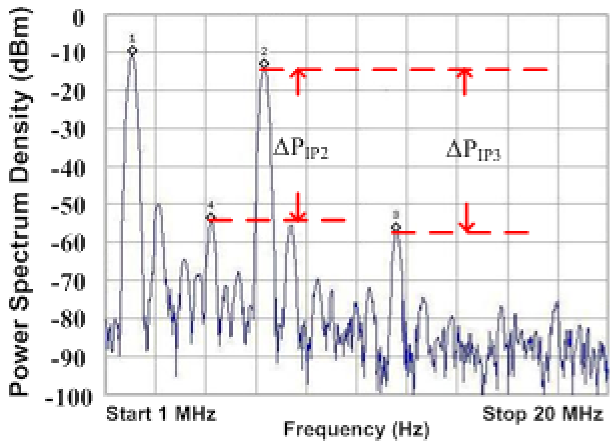
P_{1dB} at 2.44GHz

- Output return loss:
  - Simulation： S11＜-13 dB
  - Measurement： S11＜-12 dB
- Output Power:
  - Linearity: 1dB gain compression **P_{1dB} is -1.72** dBm at 2.44GHz
  - Conversion gain **16dB**
  - Power dissipation **8.88 mW** with **1.2 V** supply voltage.

RF Receiver Measurement Result



Gain compress and output power



Two tone test

$$IIP_n = P_{in} + \frac{\Delta P}{n-1}$$

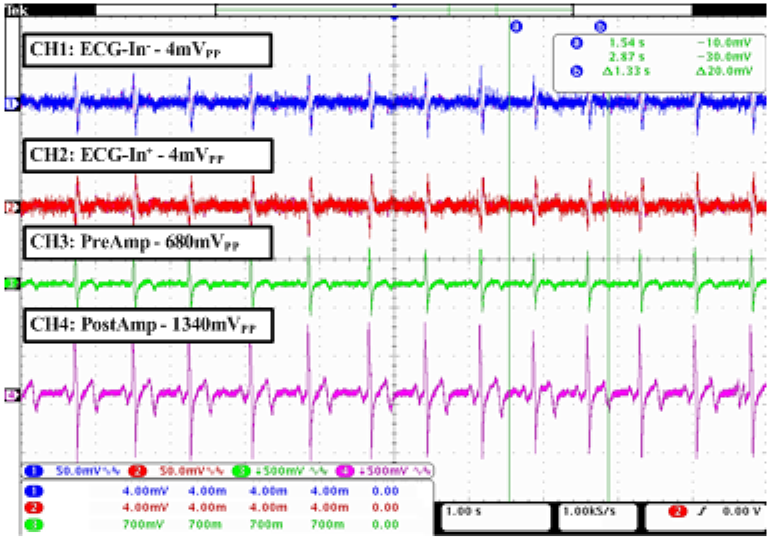
- One-tone test
  - Input return loss **-17dB** over the entire 2.4 GHz band.
  - 1 dB compression point (IP_{1dB}) **-20 dBm** with a conversion gain of **20.5 dB**.
  - Power consumption **1.14mW** and Noise Figure 13.2dB
- Two-tone test
  - Intermodulation distortion (IIP3) of **-7.8 dBm** which ZigBee SPEC **>-10 dBm**.

Summary: Receiver RF Front-end

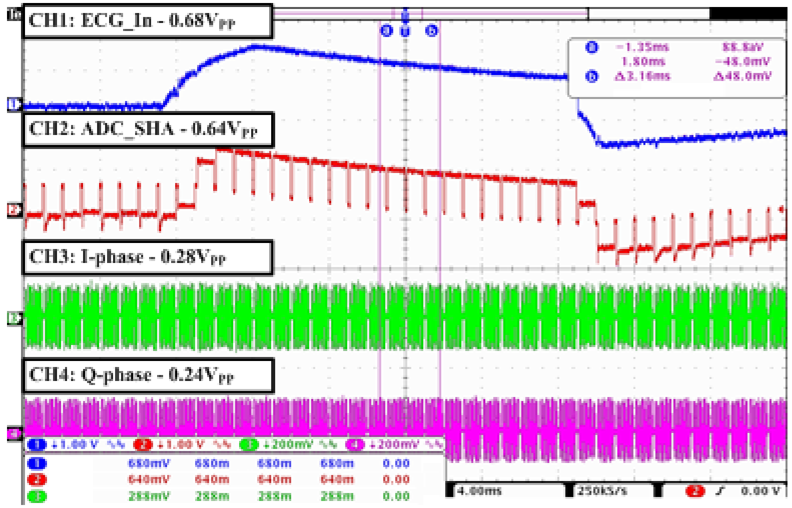
Receiver Items	ZigBee Specifications	Simulation Results	Measurement Results
S11 [dB]	NA	< -20	< -17
Conversion Gain [dB]	NA	21.4	20.5
Noise Figure [dB]	< 20.5	6.8	13.2
P1dB	> -20	-19	-20
IIP3 [dBm]	> -10	-10	-7.8
IIP2 [dBm]	> 10.5	29.4	13.5
LO-IF Leackage [dB]	NA	85	53
DC Current [uA]	NA	915	900
Power Consumption [mW]	NA	1.1	1.14

S. Y. Lee, et. al.” A Low-Power RF Front-End with Merged LNA, Differential Power Splitter, and Quadrature Mixer for IEEE 802.15.4 (ZigBee) Applications” ISCAS 2012

Real Human Body ECG Detection

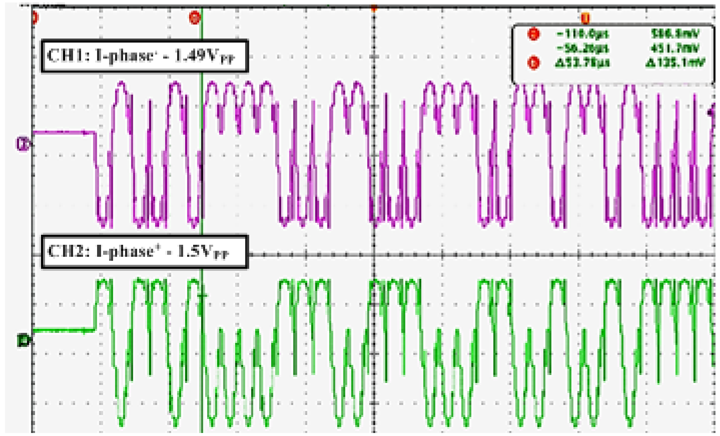


Real ECG signal



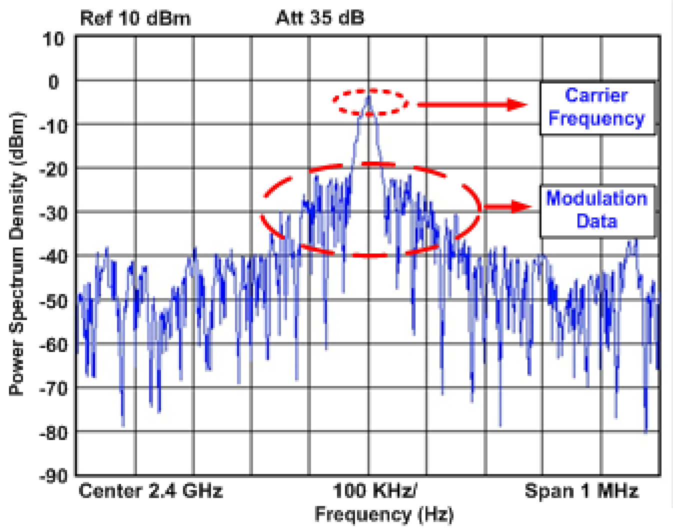
Outputs of AFE

- Blue: $4mV_{R\text{-}S}$ I/P Signal Vin^{+}
- Red: $4mV_{R\text{-}S}$ I/P Signal Vin^{-}
- Green: $680mV_{R\text{-}S}$ PreAmp O/P
- Purple: $1340mV_{R\text{-}S}$ PosAmp O/P
- Conversion gain of PGA and post-amp are 44.6dB and 50.5dB

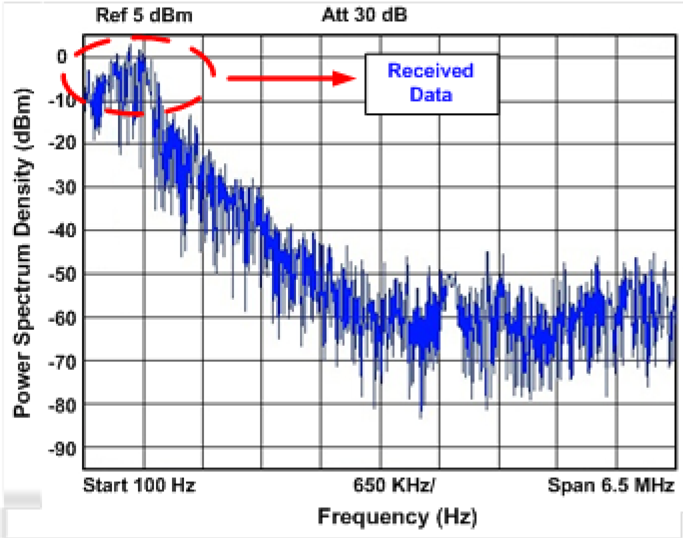


Outputs I-phase differential waveform

Data Transmission with transmitter and Receiver



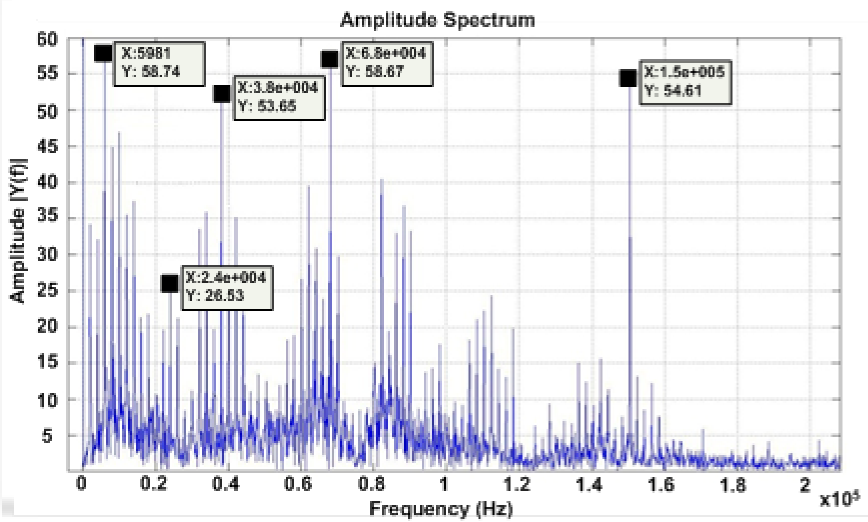
Transmitter



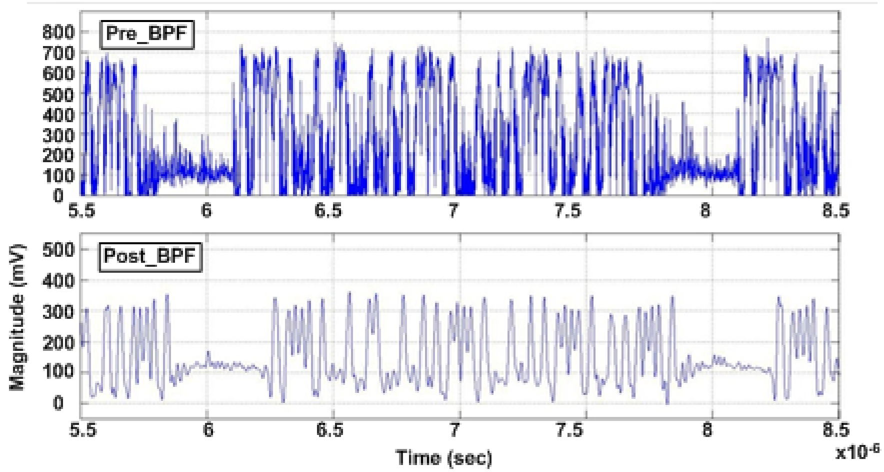
Receiver

- Transmitter
  - Power spectrum analyzer, Agilent PSA E4440A
  - Carrier frequency and data BW are **2.4 GHz and 200 KHz**, respectively.
- Receiver
  - The curve was decreased slowly until the frequency band is larger than **2.6 MHz**
  - The most amounts of data were concentrated during **150 kHz to 750 KHz**

Data Transmission with transmitter and Receiver



Received data with FFT procession

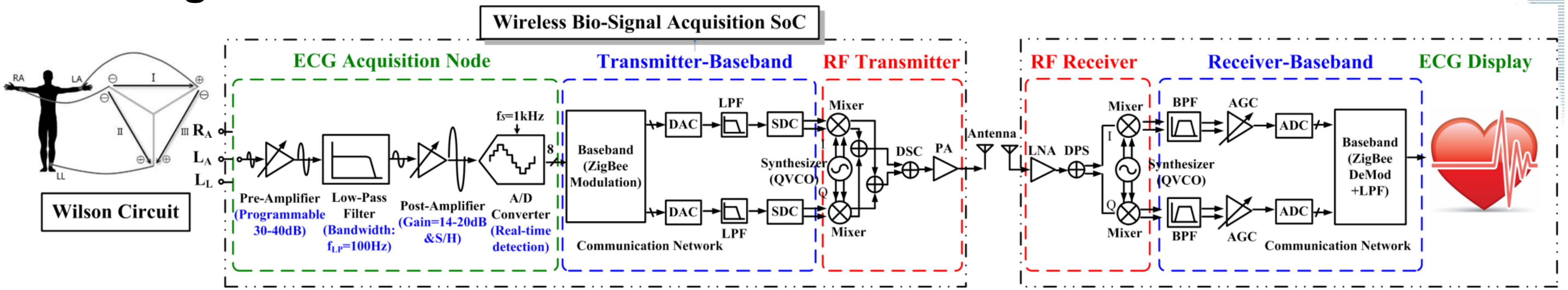


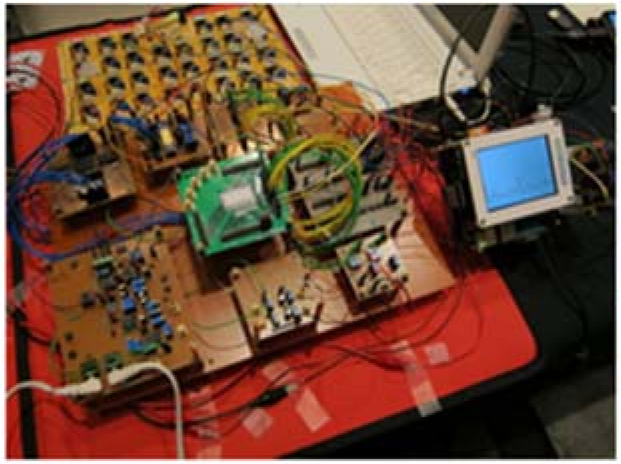
Received data of Pre_BPF and Post_BPF

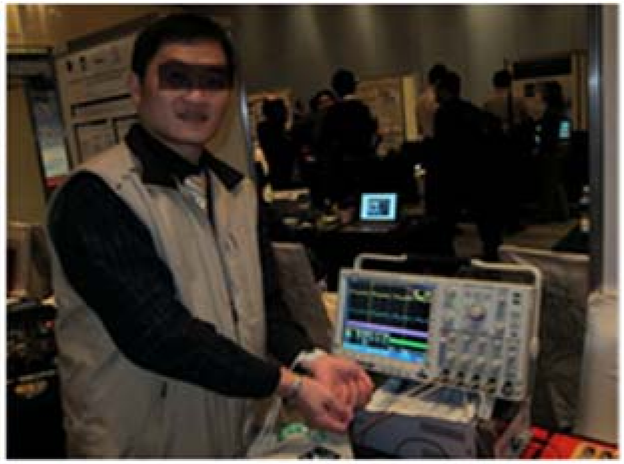
- FFT
  - Matlab simulator with fast Fourier transform (FFT) algorithm
  - The BW of the modulation data is less than 250 KHz,
  - Data distributed beside the **250 KHz**:
    - Harmonic signal and high frequency interference.
- Received Data
  - Pre_BPF vs. Post_BPF

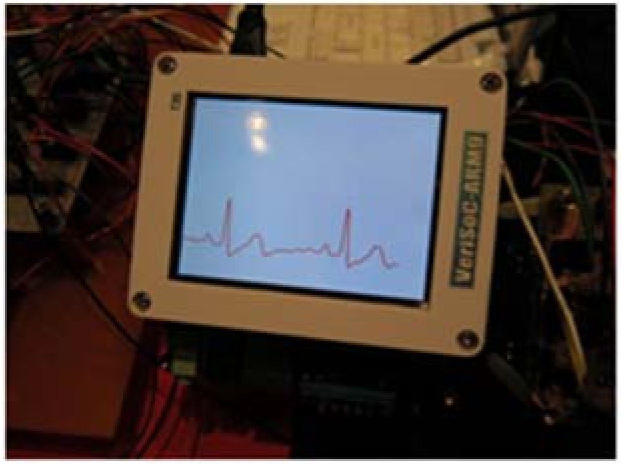
Demo Platform

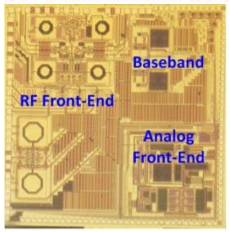
- **ZigBee transceiver**

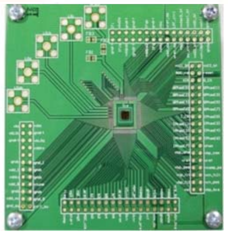












Q & A

Thanks for Your Attentions !