



系統晶片設計與應用

國立勤益科技大學 電子工程系 林光浩

Outline



- 1 **Integrated Circuit**
- 2 **Chip Design**
- 3 **Application**

Hardware Implementation



Methods or Algorithms can be implemented with

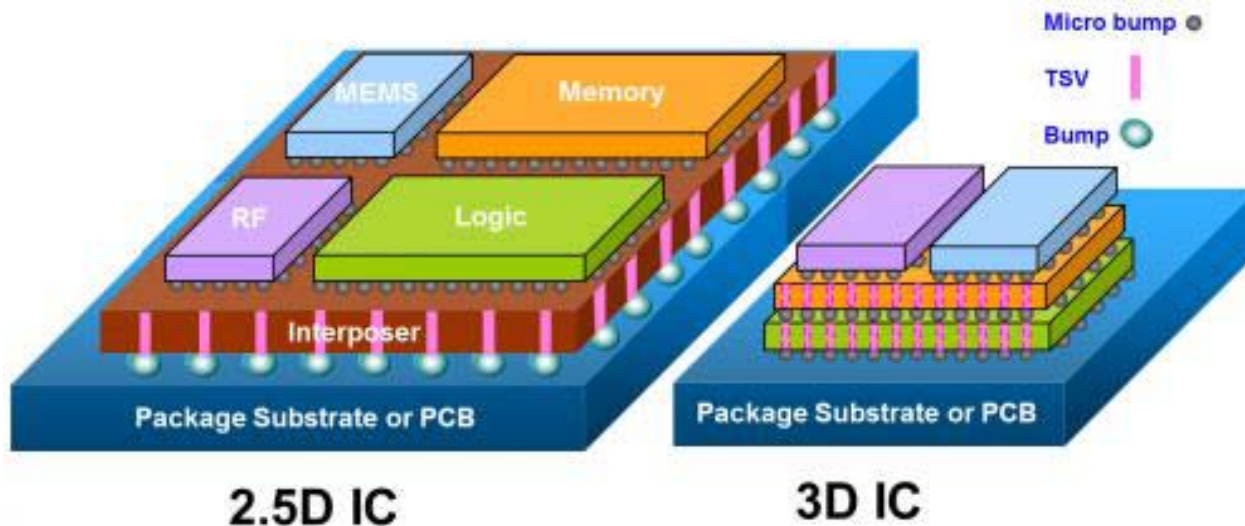
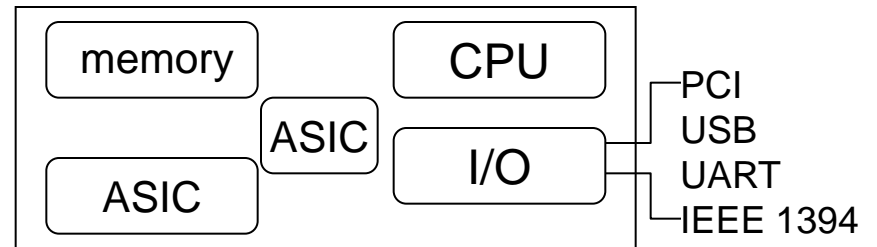
1. Hardware processor + suitable software programs (flexibility)
 - a. Pentium IV + suitable software programs (high-level language)
 - b. TI-DSP + suitable software programs
 - c. MCU(8051) + suitable software programs (low-level language)
2. Dedicated hardware circuits (faster)
 - a. old_PCBs (TTL SSI, MSI chips and wires)
 - b. new_PCBs(some devices, application specific integrated circuit-ASIC, wires)



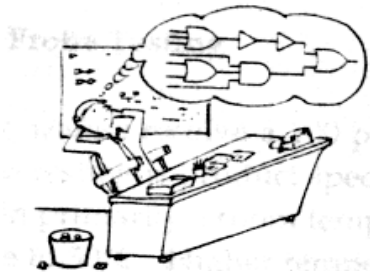
Hardware Implementation



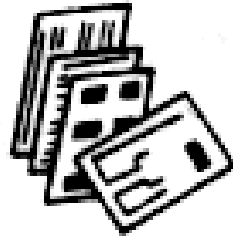
- 3. Some hardware circuits + software programs (to solve more complex problems)
 - a. System on a board (memory, processor, ASIC, I/O, other devices)
 - b. System on a chip (SoC)
 - c. current and future work (3D IC)



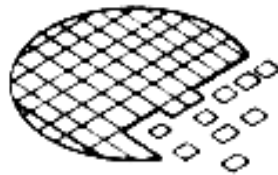
IC Industry in Taiwan



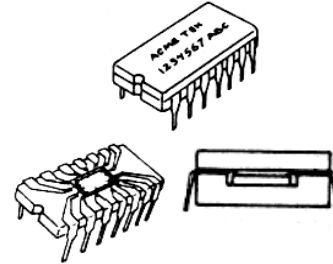
邏輯設計



光罩設計



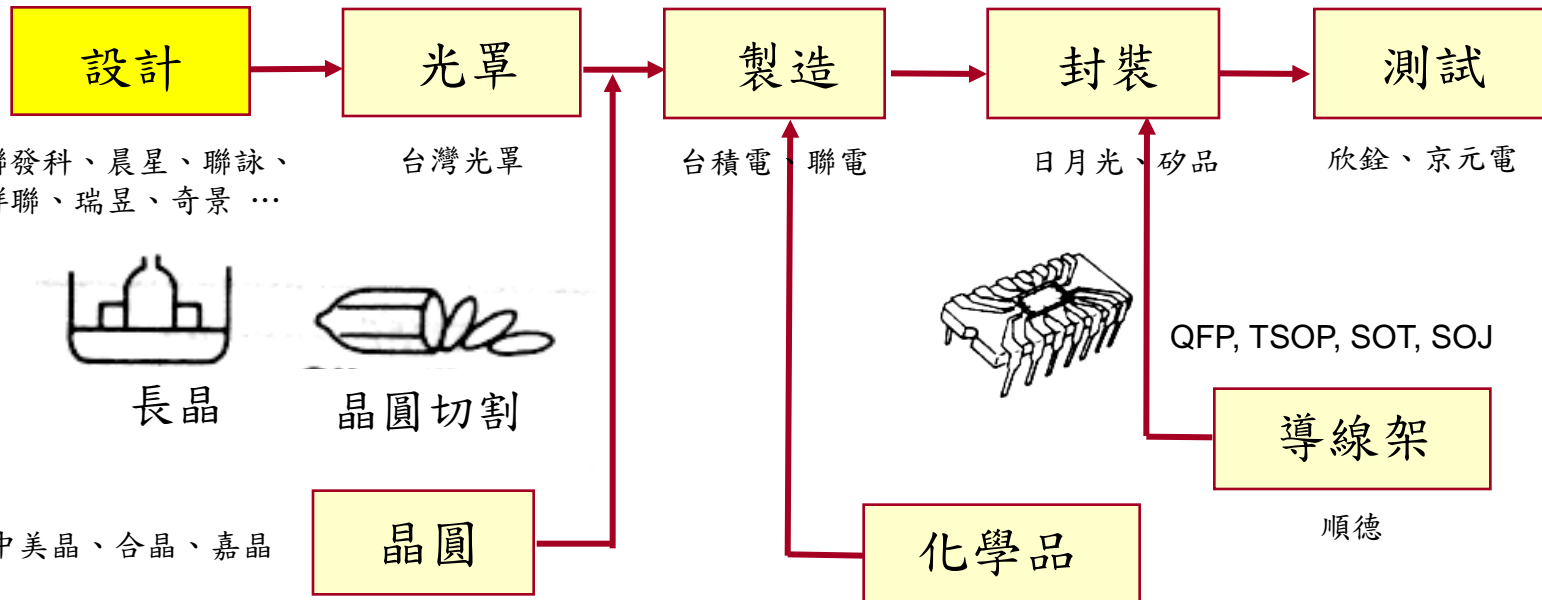
晶粒測試及切割



封裝



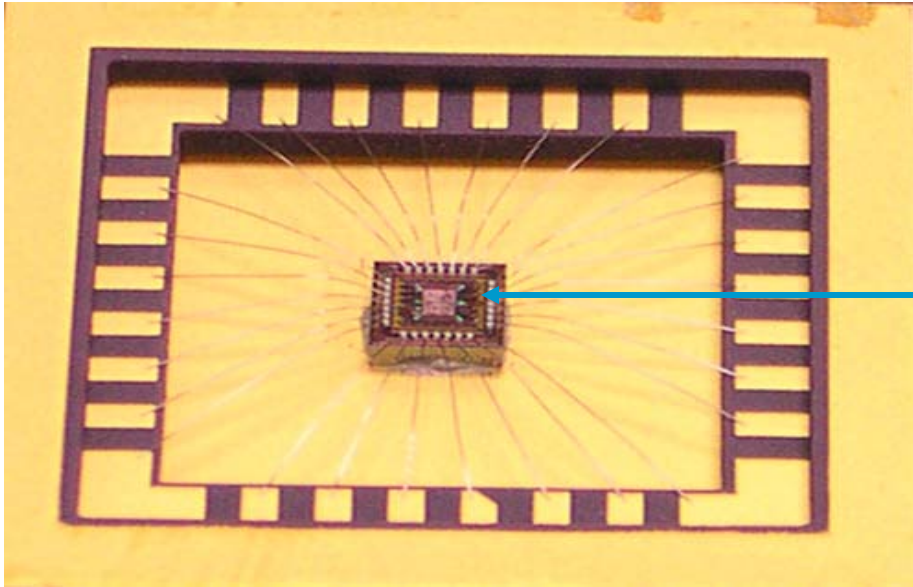
成品測試



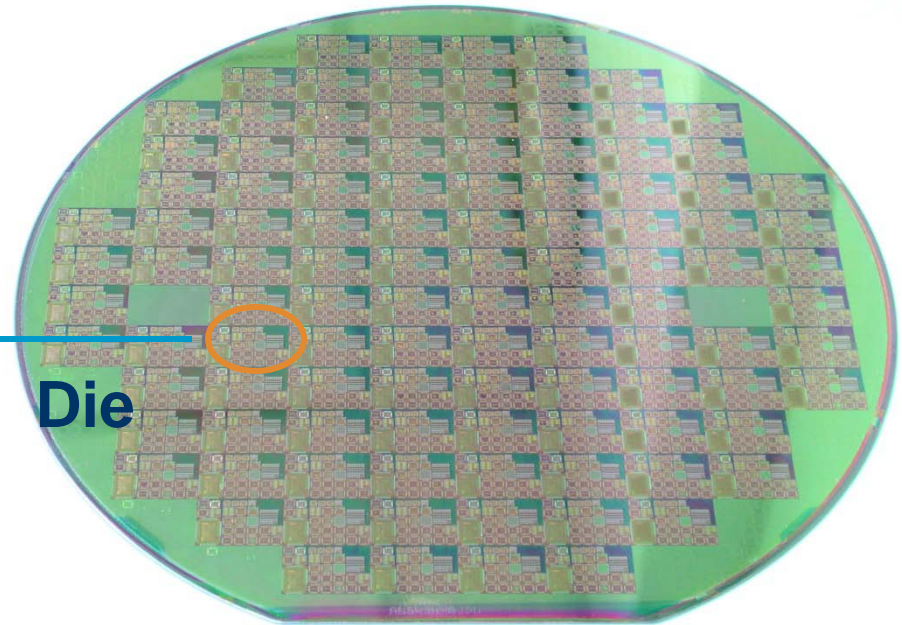
Wafer & Die & Packaging



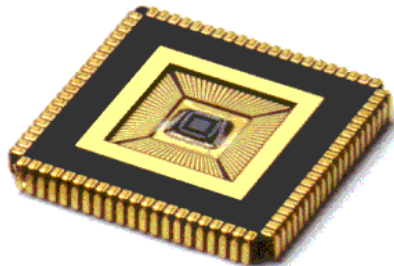
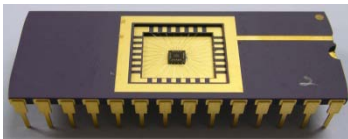
Packaging



Wafer



Die



Outline

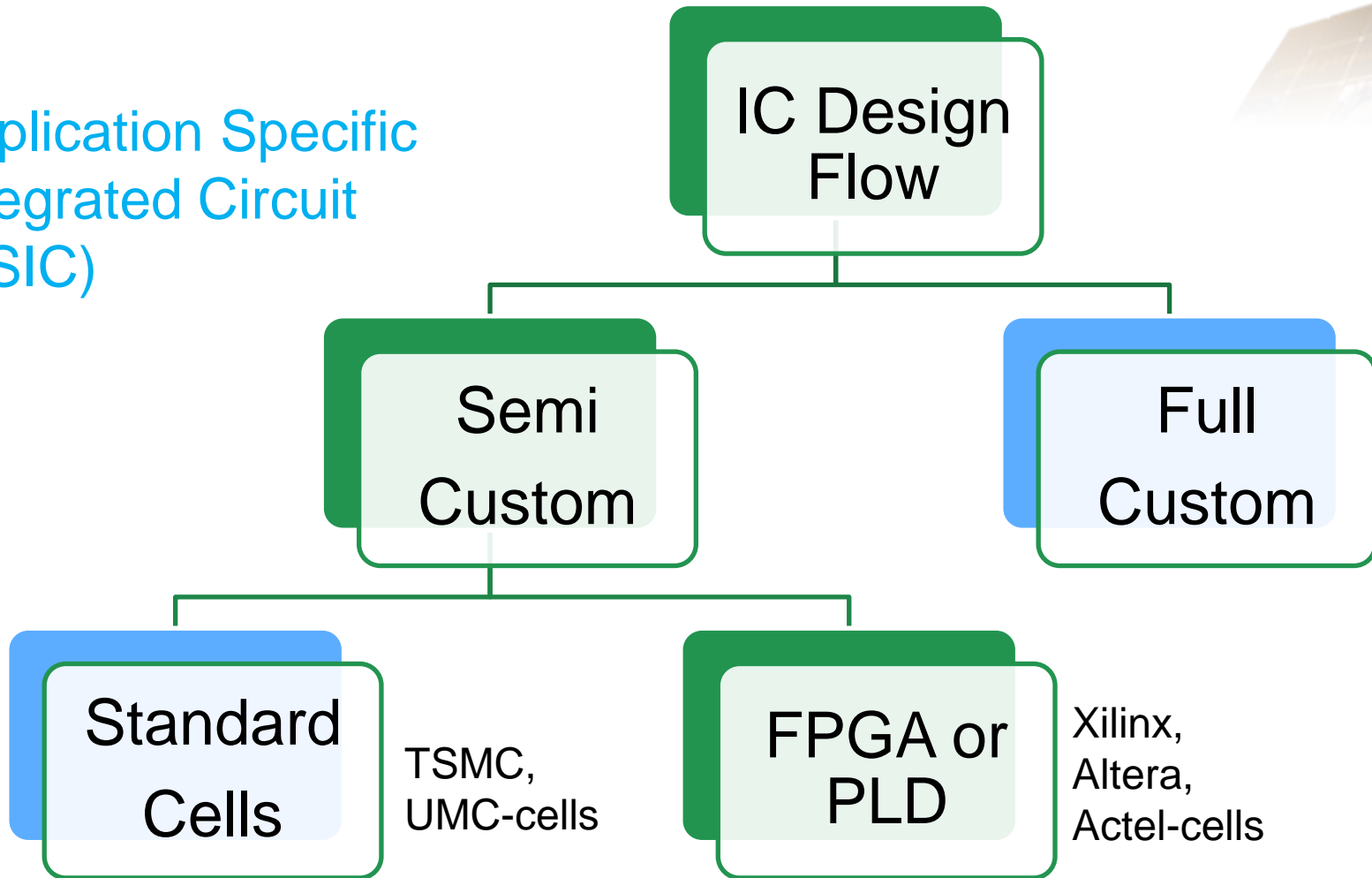


- 1 Integrated Circuit
- 2 Chip Design
- 3 Application

IC Design Flow



Application Specific
Integrated Circuit
(ASIC)



Full (Fully) Custom Design



- ❖ For analog circuits and digital circuits requiring custom optimization
- ❖ Gates, transistors and layout are designed and optimized by the engineer
- ❖ Full custom layout editor with [Virtuoso](#)

Full (Fully) Custom Design (Cont.)



Virtuoso® Schematic Editing: LTE_RFIC RX_LNA schematic

Cmd: Sel: 0

Tools Design Window Edit Add Check Sheet Options Migrate Calibre Help

mouse L: schSingleSelectPt() M: schHiMousePopUp() R: schZoomFit(1.0 0.9)

Virtuoso® Layout Reading: LTE_RFIC RX_LNA layout

X: -42.25 Y: 196.56 (F) Select: 0 DRD: OFF dX: dY: 6

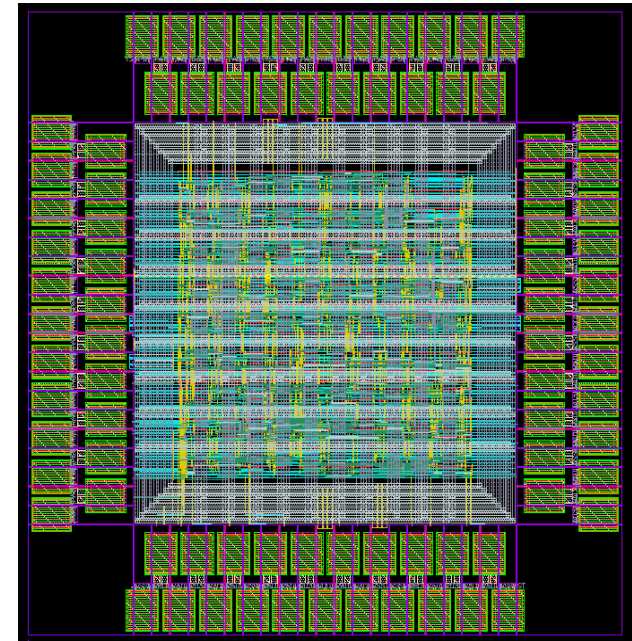
Tools Design Window Create Edit Verify Connectivity Options Routing Calibre Help

mouse L: mouseSingleSelectPt M: leHiMousePopUp() R: hiZoomAbsoluteScale(hiG)

Semi Custom Design



- ❖ For larger digital circuits
- ❖ Real gates, transistors and layout are synthesized and optimized by related software tools
- ❖ Realization with hardware description language (HDL) such as VHDL and Verilog



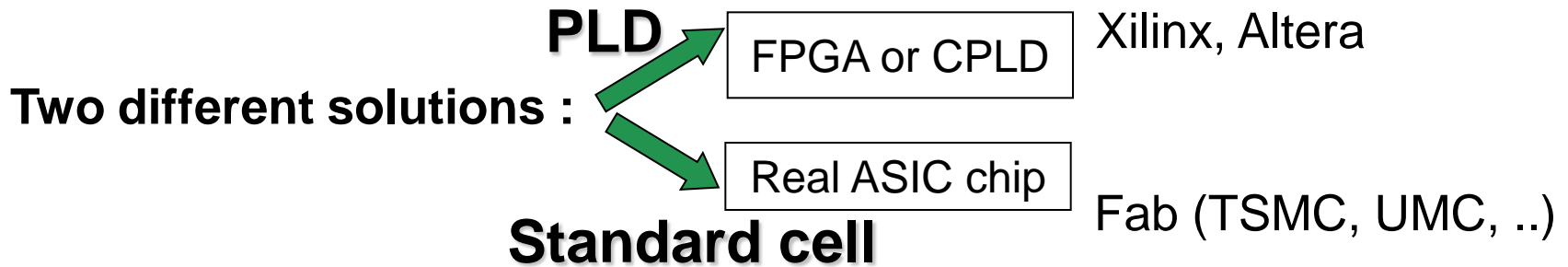
Semi Custom Design (Cont.)



- a. Product specification
- b. Modeling with HDL
- c. Synthesis (by using suitable standard cell)
- d. Simulation and verification
- e. Physical placement and layout
- f. Tape-out (real chip) -- implemented by suitable Fabrication companies
- g. Testing -- implemented by suitable tools and mechanisms

-- implemented with suitable tools

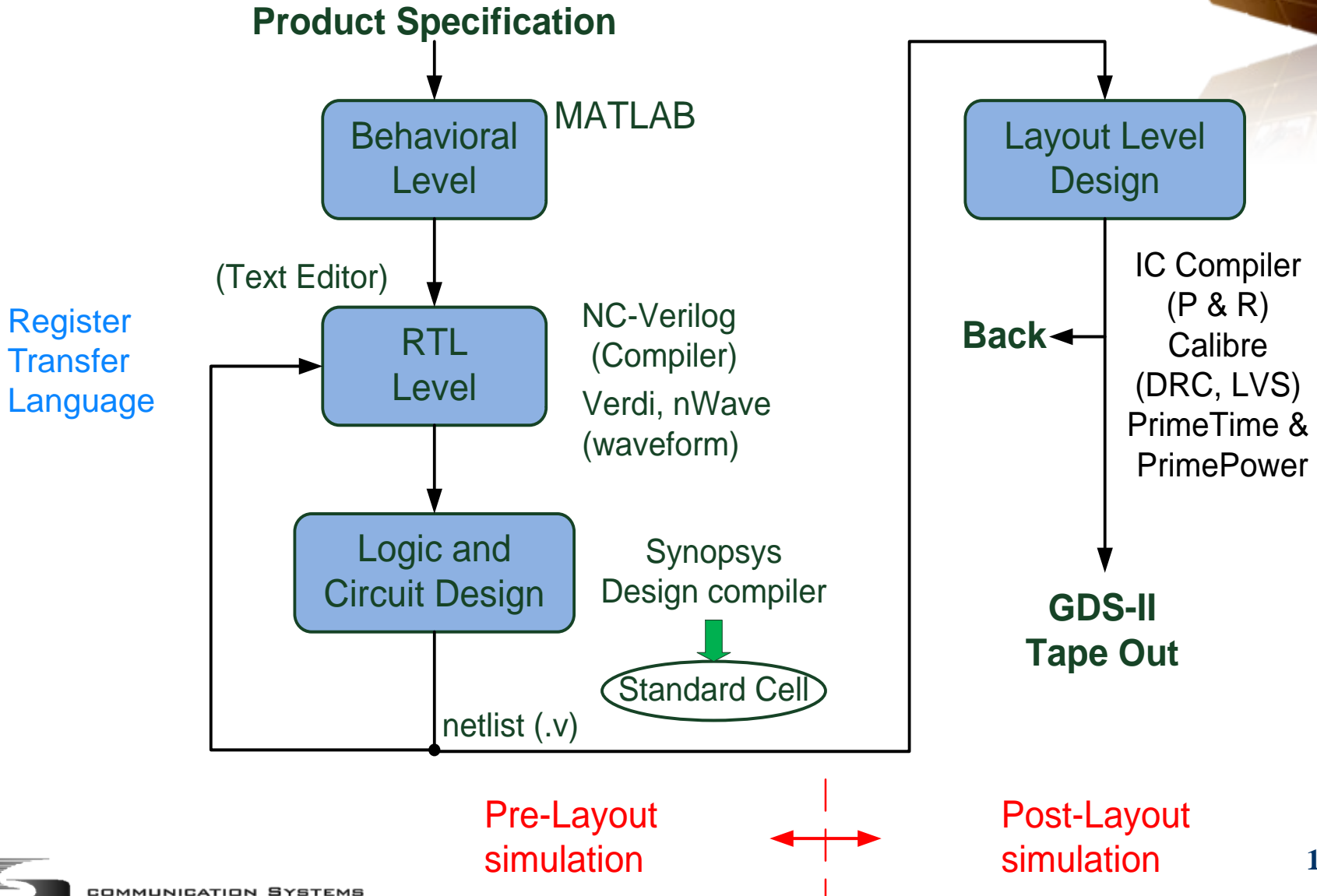
more flexible, shorter design cycle, suitable for smaller production

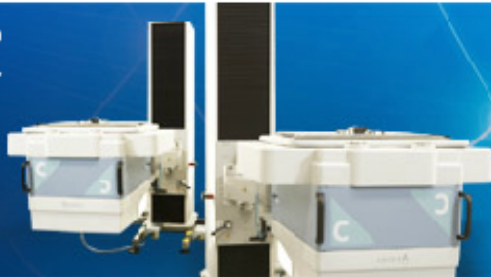


less flexible, long design cycle, larger-scale production to reduce price



Standard Cells





關於 CIC

設計服務

製程服務

量測服務

教育訓練

技術推廣

網路資源

即時訊息

會員專區

By Functionality

By Vendor

申請須知

- Vendor Package

- ◆ [- Cadence All](#)
- ◆ [- Mentor All](#)
- ◆ [- Synopsys All](#)

Cell Library

- ◆ [Cell-Based Design Kit for IC Contest](#)

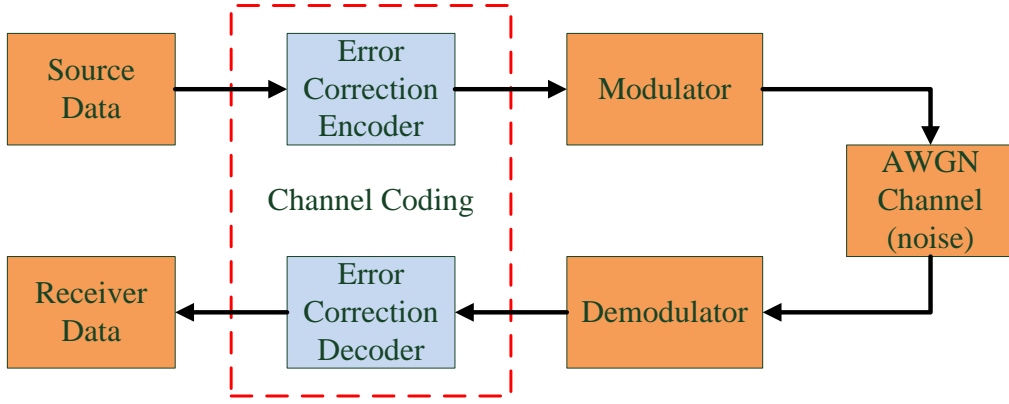
AMS Verification

- ◆ [Analog/Mixed Signal Design Flow](#)
- ◆ [Eldo](#)
- ◆ [HSPICE](#)
- ◆ [NanoSim](#)
- ◆ [SMASH](#)
- ◆ [Virtuoso Multi-Mode Simulation](#)
- ◆ [Virtuoso Spectre Circuit Simulator](#)

Custom IC Design

- ◆ [CosmosScope](#)
- ◆ [Custom Designer](#)
- ◆ [Laker Advanced Design Platform](#)
- ◆ [Laker Custom Layout Automation System](#)
- ◆ [SpiceExplorer](#)
- ◆ [Virtuoso AMS Designer](#)
- ◆ [Virtuoso Analog Design Environment](#)
- ◆ [Virtuoso NeoCircuit](#)
- ◆ [Virtuoso Schematic Editor](#)

System Simulation



System Block Diagram

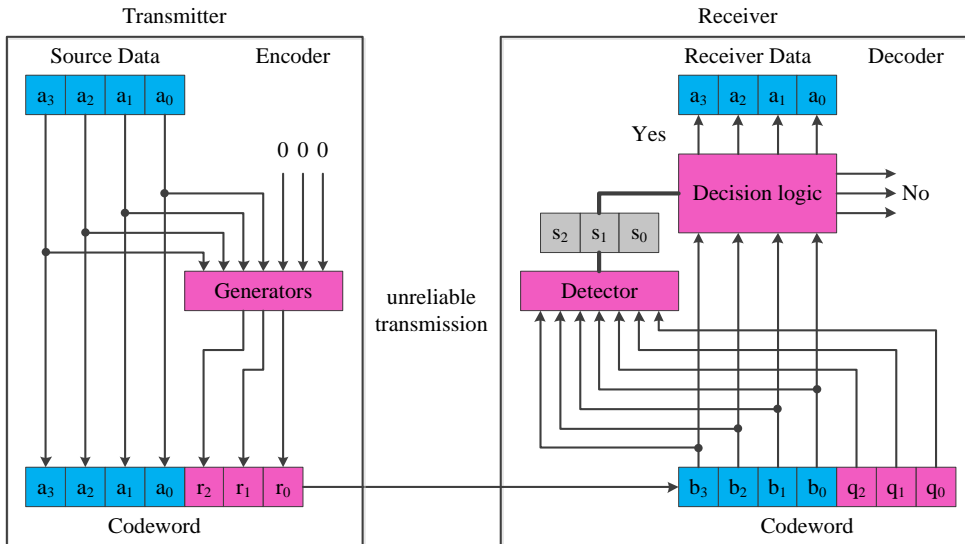
$$c(X) = c_0 + c_1X + c_2X^2 + \dots + c_{n-1}X^{n-1}$$

$$X^i c(X) = X^i(c_0 + c_1X + \dots + c_{n-i-1}X^{n-i-1} + c_{n-i}X^{n-i} + \dots + c_{n-1}X^{n-1})$$

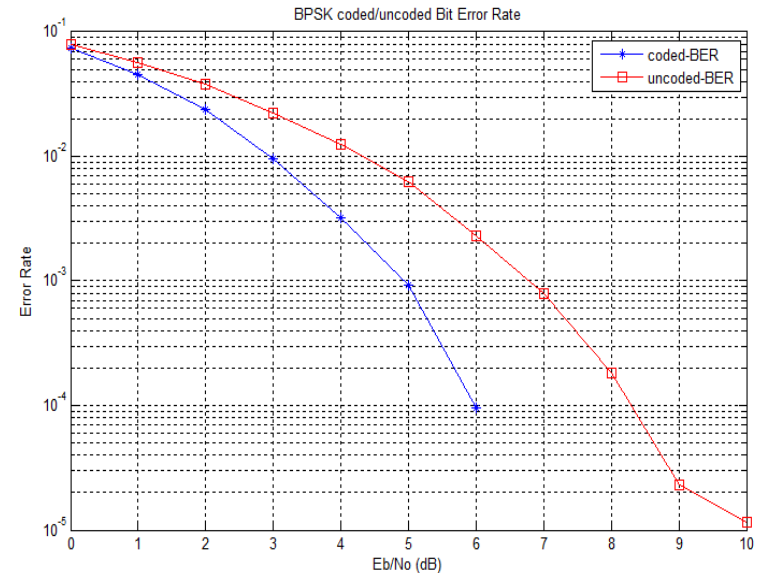
$$= c_0X^i + c_1X^{i+1} + \dots + c_{n-i-1}X^{n-1} + c_{n-i}X^n + \dots + c_{n-1}X^{n+i-1}$$

$$= c_{n-i}X^n + \dots + c_{n-1}X^{n+i-1} + c_0X^i + c_1X^{i+1} + \dots + c_{n-i-1}X^{n-1}$$

Algorithms



Circuit Architecture



Simulation Result 15

RTL Simulation



- ❖ Describe the circuits with Hardware Description Language (HDL) – **Verilog-HDL**, **VHDL**
- ❖ Verification and Analysis
 - **Behavioral Simulation**
 - **Logic Simulation**
 - **Circuit Simulation**
- ❖ ModelSim – Supported on Windows and Linux operating systems
- ❖ Verdi – Supported on Linux operating system

ModelSim

SYNOPSYS[®]
Accelerating Innovation



ModelSim



ModelSim SE PLUS 6.2f

File Edit View Compile Simulate Add Wave Tools Layout Window Help

Workspace

| Name | Status |
|-----------------|--------|
| FIR_filter_tb.v | ✓ |
| adder_8.v | ✓ |
| adder_1.v | ✓ |
| DFF8.v | ✓ |
| mul_8.v | ✓ |
| FIR_filter.v | ✓ |

Objects

| Name | Value |
|-------|--------|
| clk | 0 |
| reset | 0 |
| xin | 000000 |
| yout | 000000 |
| i | 256 |

wave - default

| Signal | Value |
|-----------------------|----------------------------|
| /FIR_filter_tb/clk | 0 |
| /FIR_filter_tb/reset | 0 |
| /FIR_filter_tb/xin | 00000000 11100010 11100011 |
| /FIR_filter_tb/yout | 00000000 00010100 |
| /FIR_filter_tb/i | 256 227 228 |
| /FIR_filter_tb/ff0... | S10 |
| /FIR_filter_tb/ff0... | S10 |
| /FIR_filter_tb/ff0... | 00000000 11100010 11100011 |
| /FIR_filter_tb/ff0... | 00000000 00010100 |
| /FIR_filter_tb/ff0... | 00000000 11100010 11100011 |
| /FIR_filter_tb/ff0... | 00000000 11100001 11100010 |
| /FIR_filter_tb/ff0... | 00000000 11100000 11100001 |
| /FIR_filter_tb/ff0... | 00000000 11011111 11100000 |
| /FIR_filter_tb/ff0... | 00000000 11011110 11011111 |
| /FIR_filter_tb/ff0... | 00000000 11011101 11011110 |
| /FIR_filter_tb/ff0... | 00000000 11011100 11011101 |
| /FIR_filter_tb/ff0... | 00000000 11011011 11011100 |
| /FIR_filter_tb/ff0... | 00000000 11011010 11011011 |
| /FIR_filter_tb/ff0... | 00000000 11011001 11011010 |
| /FIR_filter_tb/ff0... | 00000000 11011000 11011001 |
| /FIR_filter_tb/ff0... | 00000000 11010111 11011000 |

Now 5650 ns
Cursor 1 0 ns

4560 4580

File Edit View Tools Window

```
1 module FIR_filter(clk,reset,xin,yout);
2 input clk,reset;
3 input [7:0] xin;
4 output [7:0] yout;
5 parameter [7:0] a0=8'b00000000,
6 a1=8'b00000000,
7 a2=8'b00000001,
8 a3=8'b11111110,
9 a4=8'b11111010,
10 a5=8'b00000000,
11 a6=8'b00010111,
12 a7=8'b00101111,
13 a8=8'b00101111,
14 a9=8'b00010111,
15 a10=8'b00000000,
16 a11=8'b11111010,
17 a12=8'b11111110,
18 a13=8'b00000001,
19 a14=8'b00000000,
20 a15=8'b00000000;
21
22 wire [7:0] xin1,xin2,xin3,xin4,xin5,xin6,xi
23 wire [7:0] xin9,xin10,xin11,xin12,xin13,xin
24 wire [15:0] p0,p1,p2,p3,p4,p5,p6,p7,p8,p9,p1
25 wire [7:0] s1,s2,s3,s4,s5,s6,s7,s8,s9,s10,s
26 wire [14:0] co;
27
28 DFF8 d1(.clk(clk), .reset(reset), .D(xin), .
29 DFF8 d2(.clk(clk), .reset(reset), .D(xin1),
30 DFF8 d3(.clk(clk), .reset(reset), .D(xin2),
31 DFF8 d4(.clk(clk), .reset(reset), .D(xin3),
32 DFF8 d5(.clk(clk), .reset(reset), .D(xin4),
```

Transcript

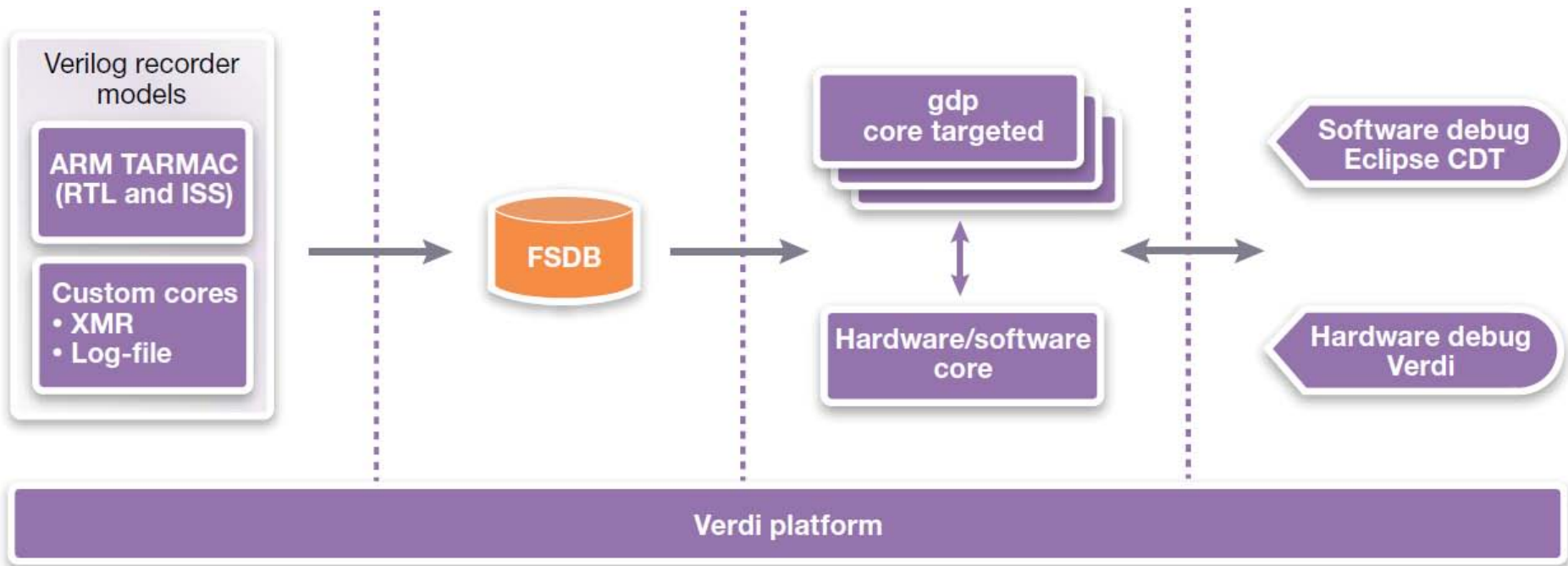
```
## Note: $finish : D:/ModelSim/DSP_filter/FIR_filter_tb.v(22)
# Time: 5650 ns Iteration: 0 Instance: /FIR_filter_tb
# 1
# Break in Module FIR_filter_tb at D:/ModelSim/DSP_filter/FIR_filter_tb.v line 22
VSIM 4>
```

Project: FIR_filter Now: 5,650 ns Delta: 0 sim:/FIR_filter_tb#INITIAL#12 Ln: 6 Col: 31

HDL Debugging with Verdi



- ❖ The Verdi system lets you focus on tasks that add more value to your designs by cutting your debug time, typically by over 50%



Ref : Synopsys Debug

<https://www.synopsys.com/Tools/Verification/debug/Pages/default.aspx>

Verilog TraceMan:1> tb_CPUsystem.i_CPUsystem.i_CPU.i_ALUB (ALUB.v) - /home1/.../cpu/src/dump.fsdb

File View Source Trace Debug Tools Window Help

By: 212 x 1ns

<Inst_Tree>

- tb_CPUsystem
 - i_BJkernel (BJkernel)
 - i_BJsource (BJsource)
 - i_CPUsystem (CPUsystem)
 - i_CPU (CPU)
 - i_ALUB (ALUB)
 - i_alu (alu)
 - i_CCU (CCU)
 - i_maprom (maprom)
 - i_mprom (mprom)
 - i_PCU (PCU)
 - i_pram (pram)

<Src:1>tb_CPUsystem.i_CPUsystem.i_CPU.i_ALUB (/home1/rich_chang/demo1/verilog/cpu/src/ALUB.v)

```

59     case (OpBusMode)
60         0:     aluInA = IXR;
61             0
62         1:     aluInA = ACC;
63             0
64         2:     aluInA = PC;
65             0
66         3:     aluInA = ACC;
67             0
68         default: aluInA = DataIn;
69             0
70     endcase
71
72 always @(OpBusMode or PC or ACC or IXR )
73     case (OpBusMode)
74         0:     aluInB = 8'h00;
75     endcase
  
```

<Inst_Tree> <Decl_Tree>

<nWave:2> /home1/rich_chang/demo1/verilog/cpu/src/dump.fsdb

File Signal View Waveform Analog Tools Window

212 0

By: Go to:

01

- a[7:0]
- b[7:0]
- cin
- select[2:0]
- out[7:0]
- carry
- zero

02

- RESET
- CLOCK1
- CLOCK2
- CLOCK3
- CLOCK4
- R_Wmode
- VMAmode

<Message> <nWave:2> dump.fsdb

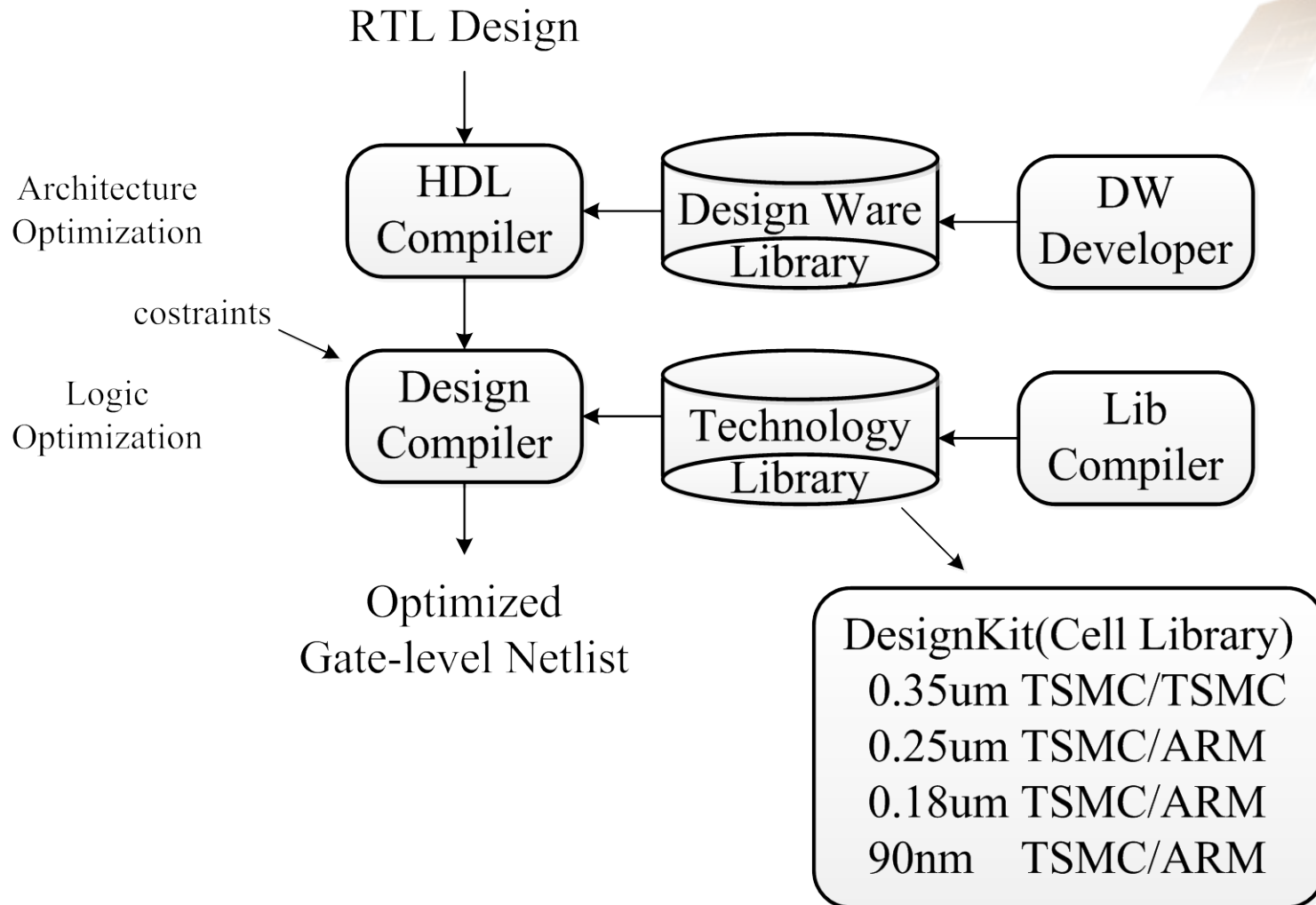
<FlowView:3> Temporal Flow View

File View Trace Tools

212 Clock: >>

WAIT op
CLOCK2
BUSV
RBSW
1

Logic Synthesis with Design Compiler



Synthesis

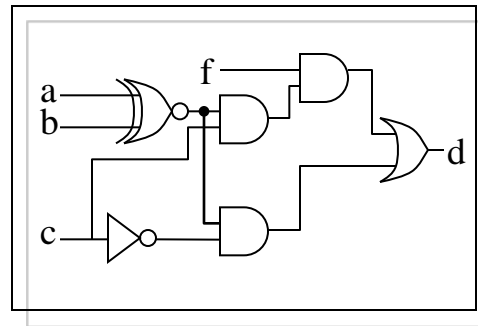


❖ *Synthesis = Translation+Optimization+Mapping*

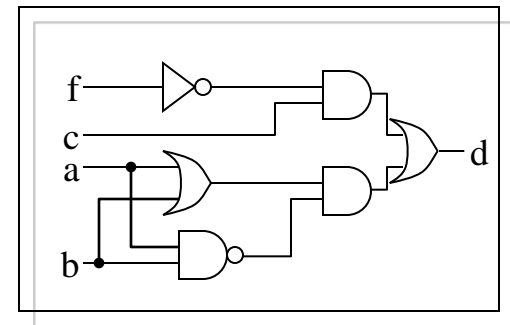
```
always @(...)  
  if (a==b)  
    if (c==1)  
      d=f;  
    else  
      d=1;  
  else  
    d=0;
```

HDL Source

Translate into Boolean Representation



Optimize + Map



Target Technology

Process of logic synthesis

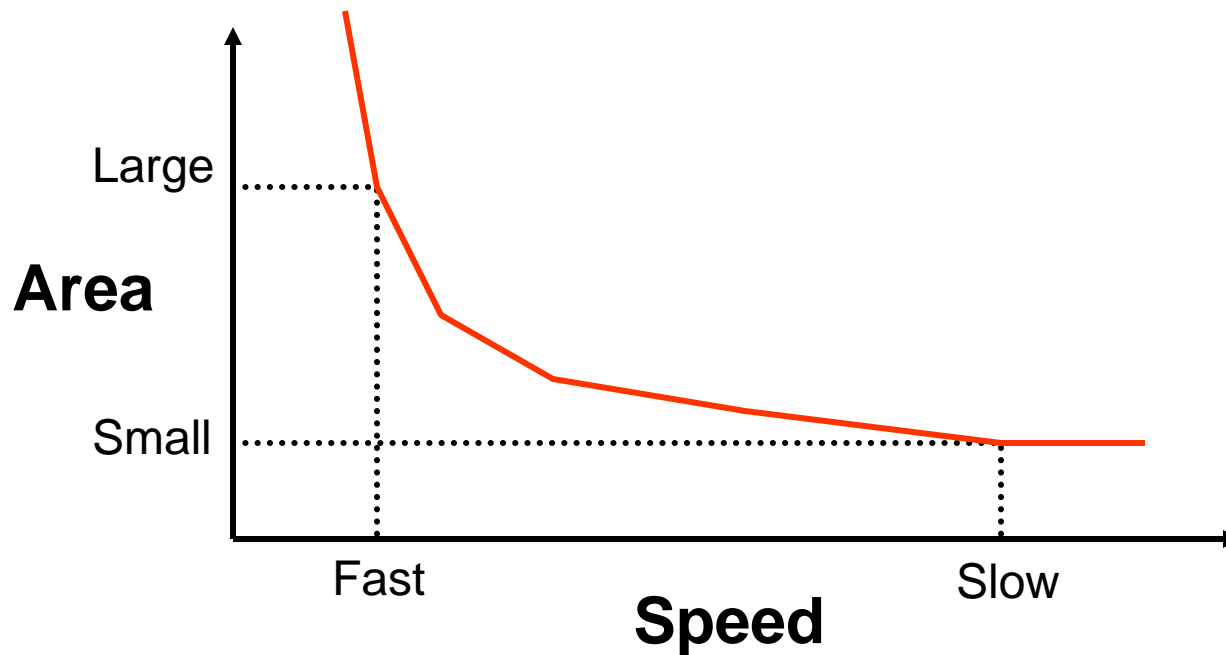


Synthesis (Cont.)



❖ Synthesis is **constraint-driven**

- You set the goals. Design Compiler optimizes design toward goals.



Synthesis (Cont.)



Design Vision - TopLevel.1 (CHIP)

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help

CHIP

Hier.1

Logical Hier Cells (Hierarchical)

| Cell Name | Ref Name | Cell Path | Di |
|-----------|----------|-----------|------|
| c1 | ECC_v4 | c1 | u... |

Report.1 - Timing

| | |
|--------------------|-------|
| data required time | 9.00 |
| | |
| data required time | 9.00 |
| data arrival time | -8.97 |
| slack (MET) | 0.03 |

***** End Of Report *****

Hier.1 Report.1

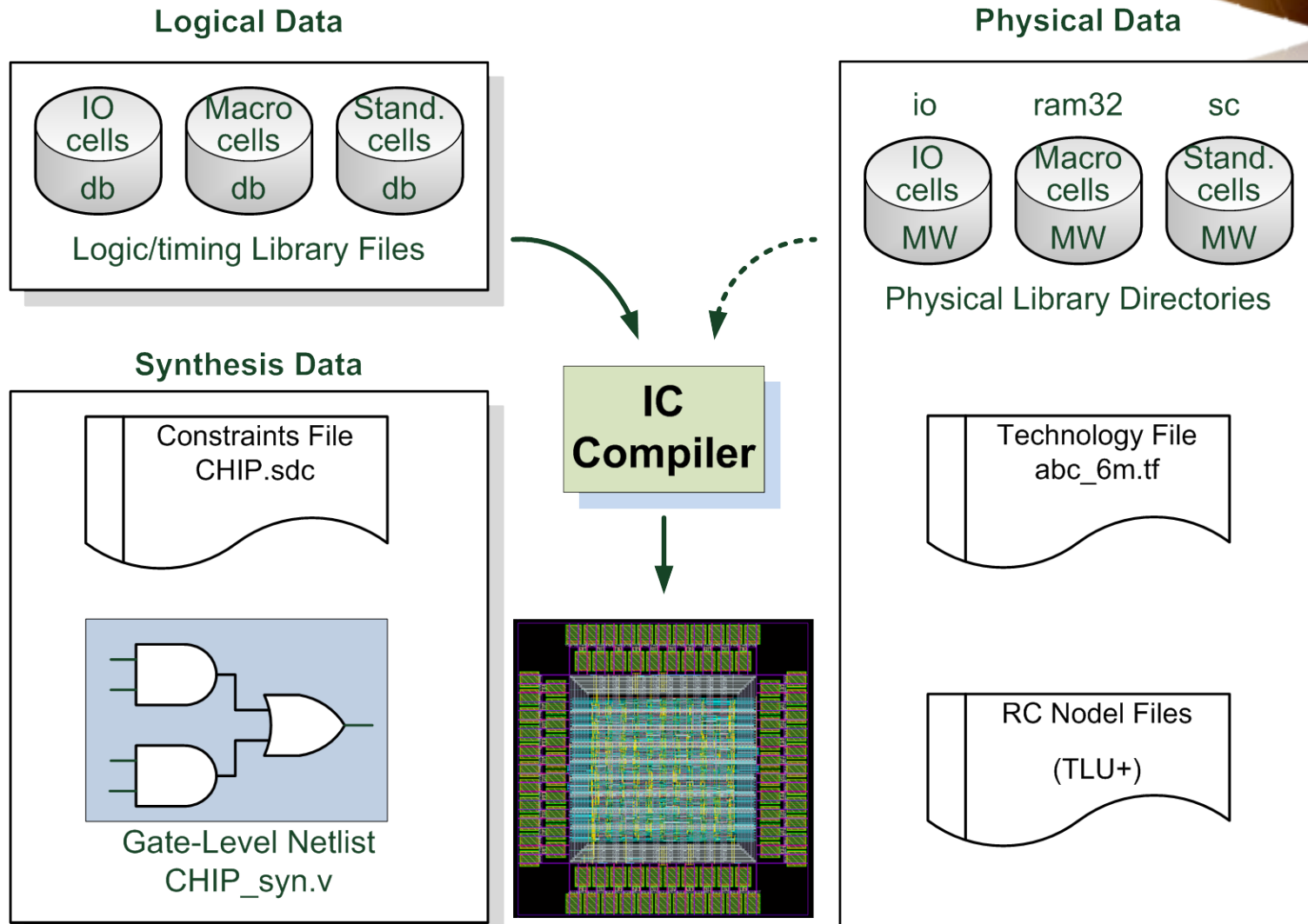
```
1
Current design is 'CHIP'.
design_vision> uplevel #0 { report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -
Information: Updating graph... (UID-83)
Information: Updating design information... (UID-85)
```

Log History Options: ▾

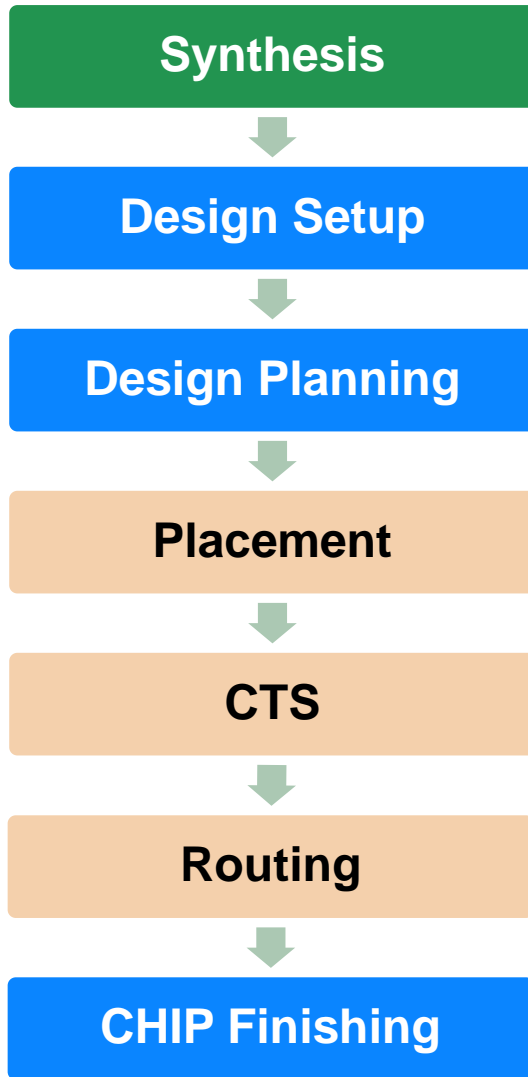
design_vision>

Ready

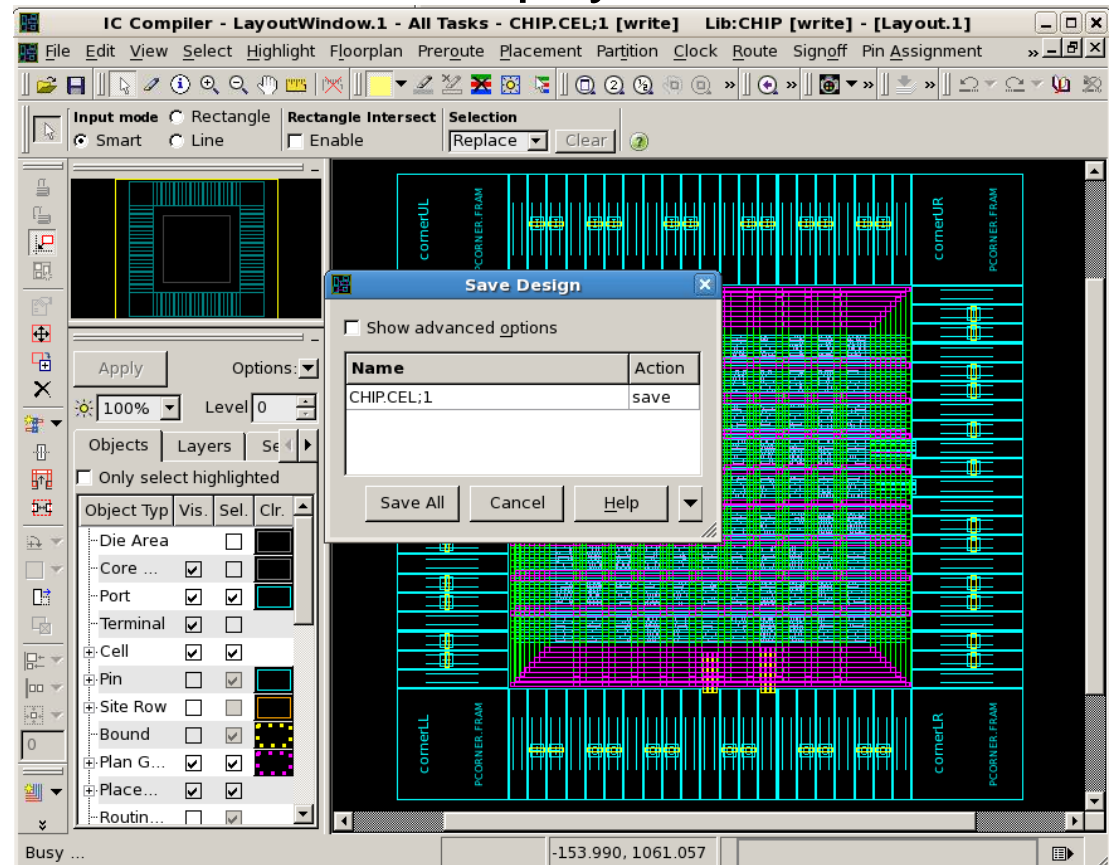
Cell-Based IC Physical Design and Verification with IC Compiler



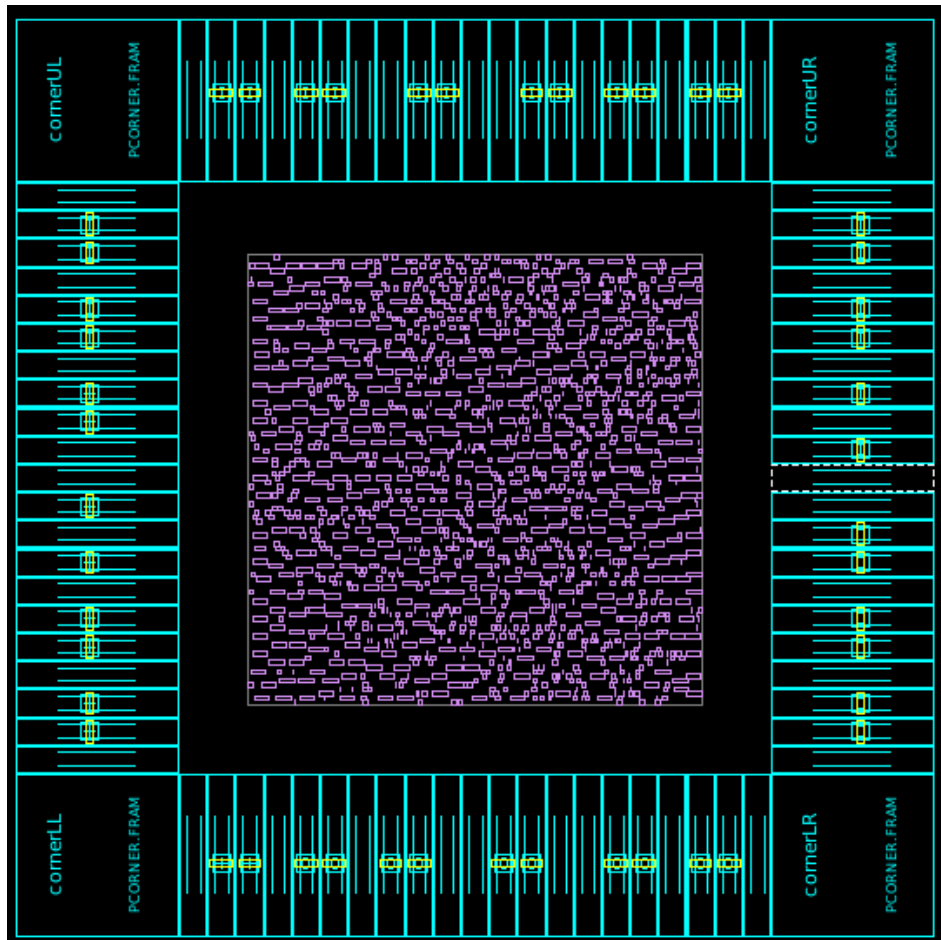
IC Compiler Flow



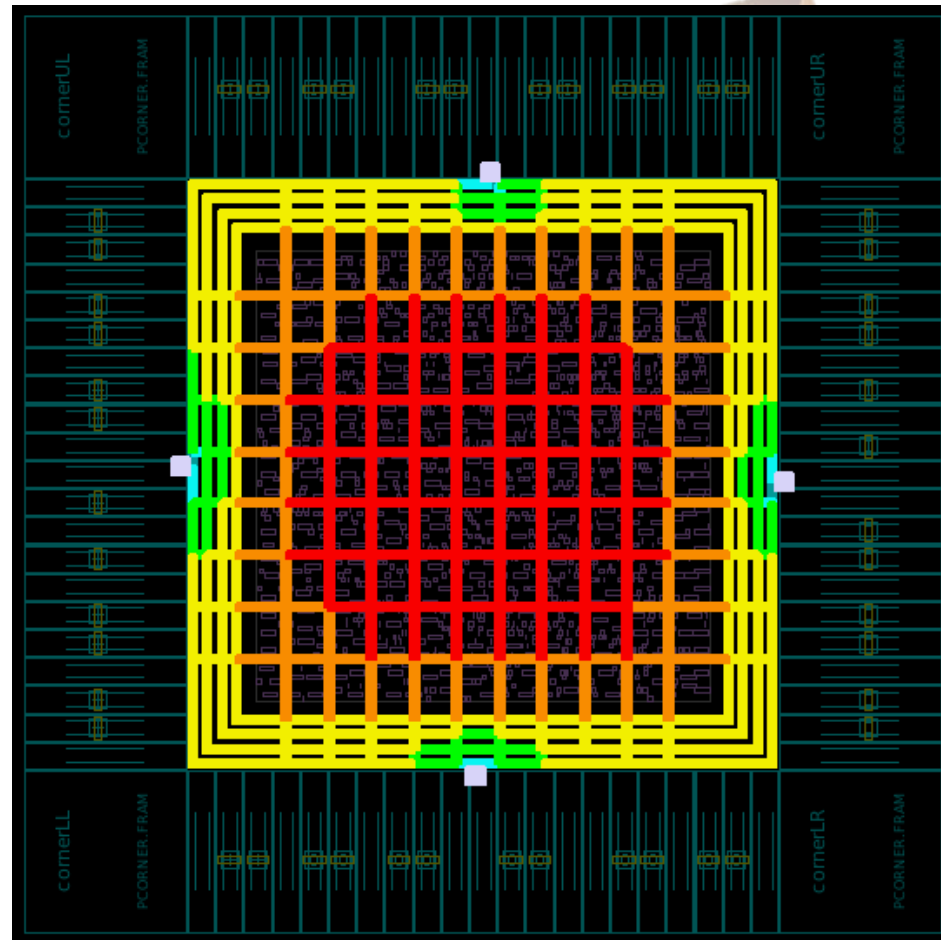
- ❖ Tcl or GUI-based user interface
- ❖ All Design Compiler reports enhanced with physical information



Placement

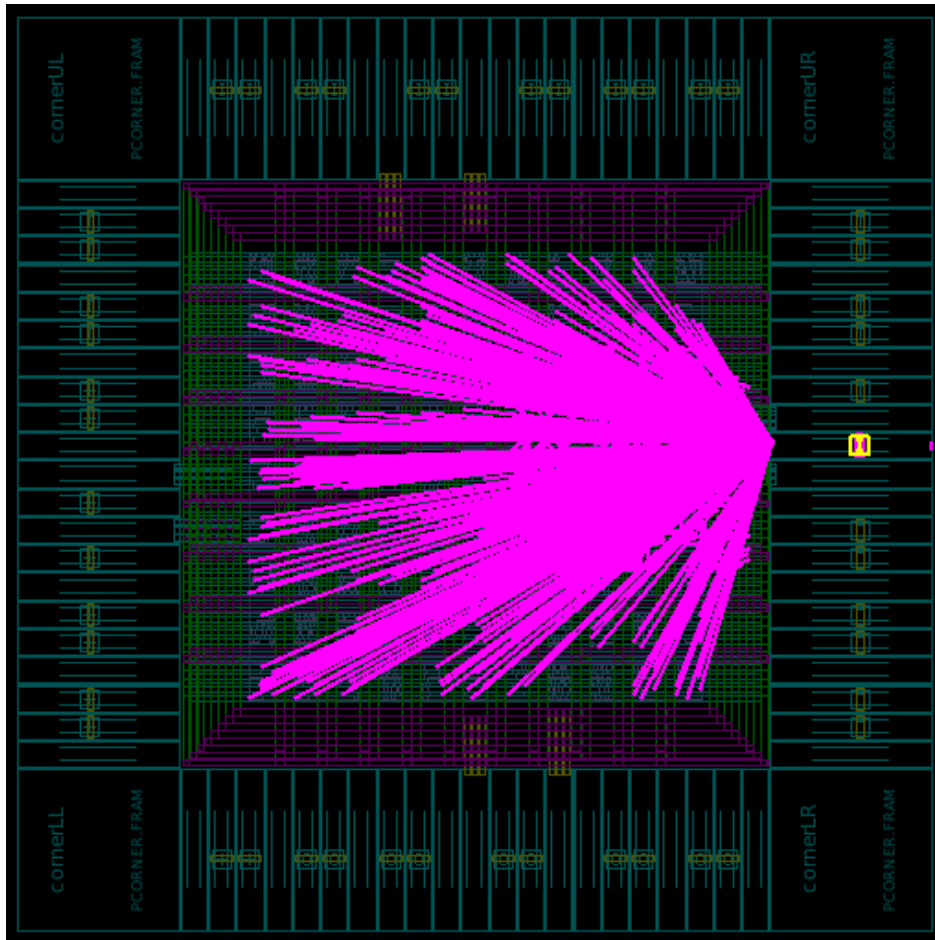


Floor plan

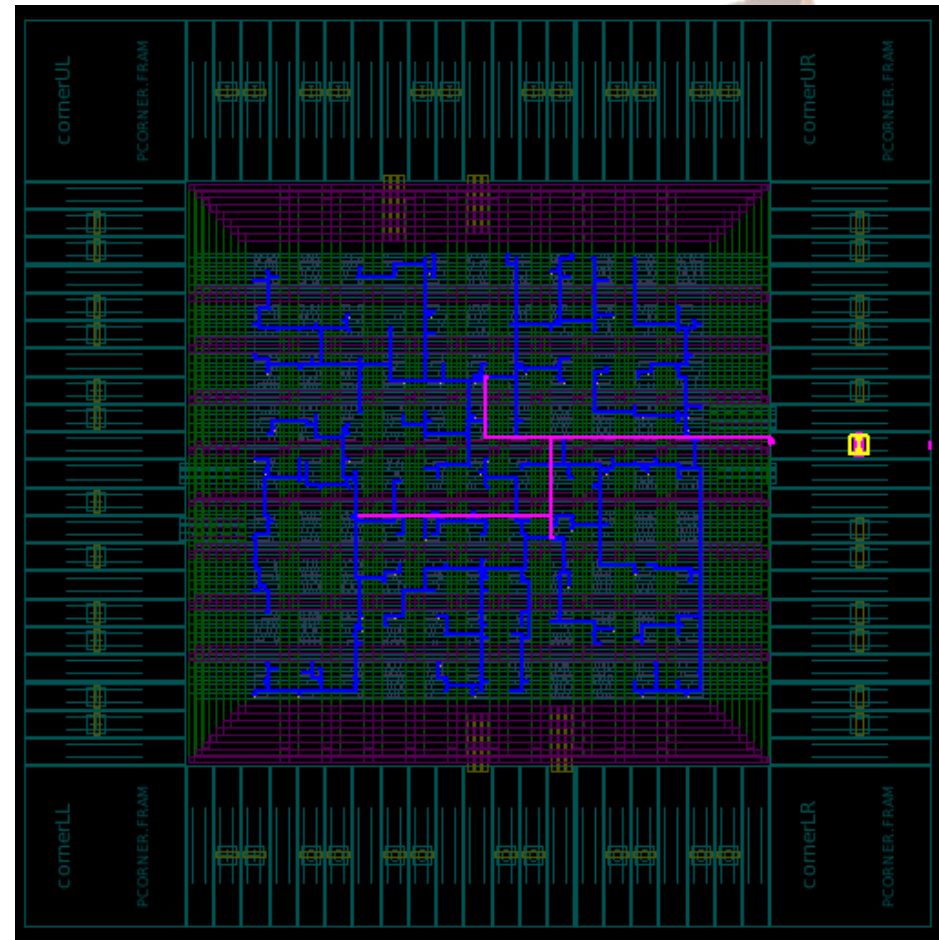


Power plan

Clock Tree Synthesis



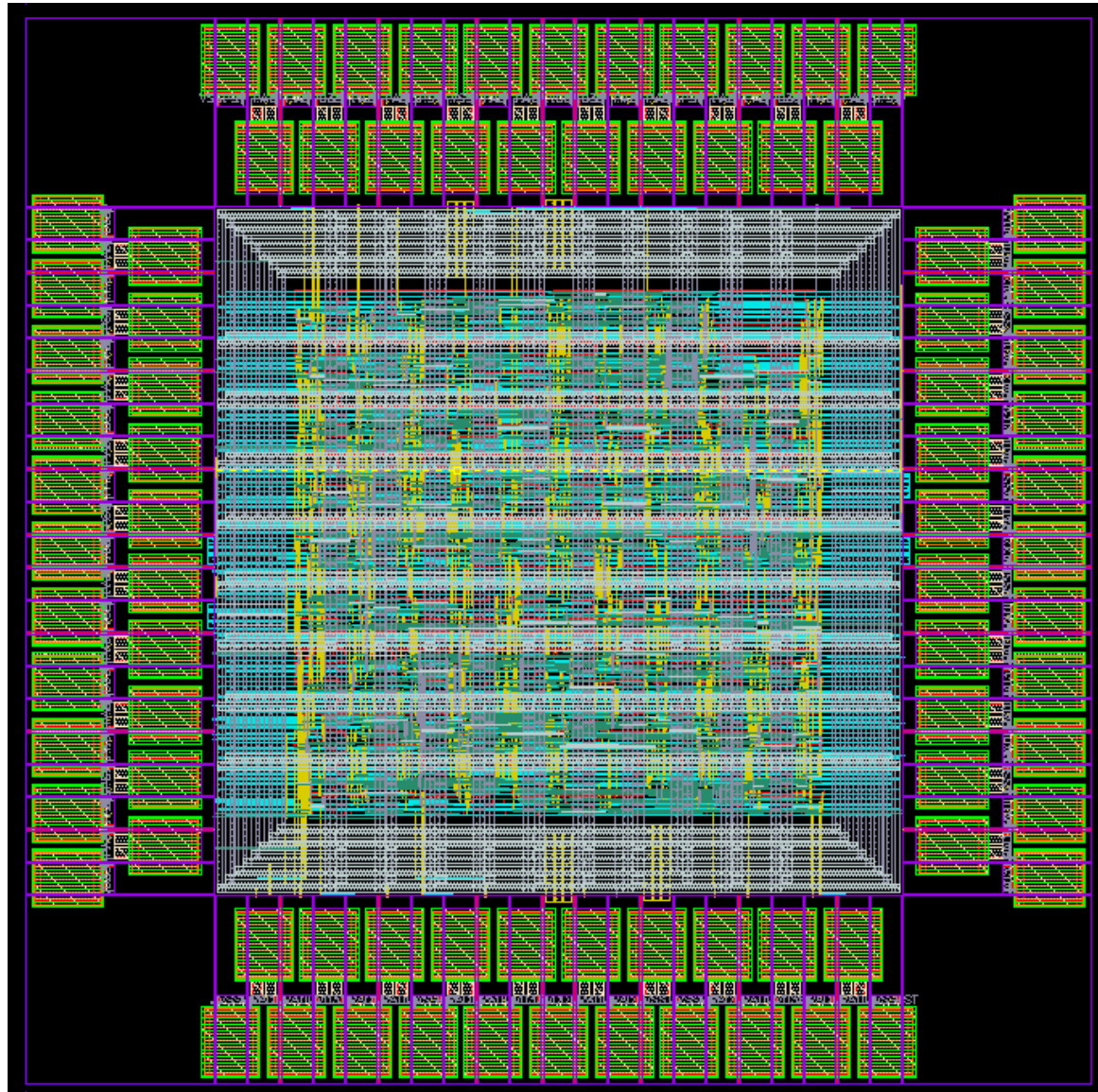
Before CTS



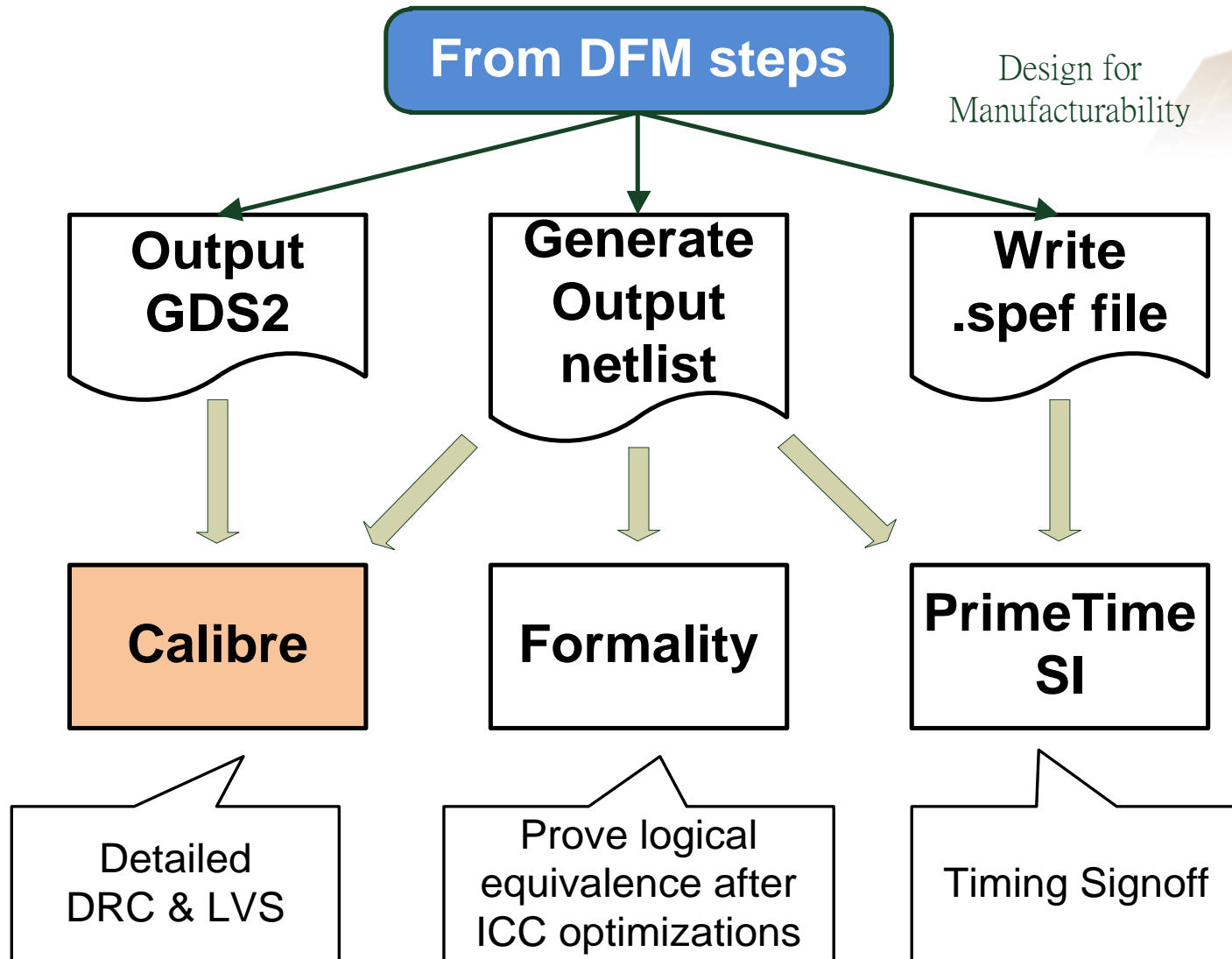
After CTS



Routing



Final Validation



Calibre



❖ Push button access to Calibre

- DRC, LVS, xRC

❖ Shorter iteration time

- Direct invocation from design environment
- Rapid verification & parasitic extraction
- Easy location of results in design environment
- Faster repair of errors & discrepancies
- Parasitic visualization

❖ Shorter time to tape-out

Design Rule Check



Calibre - RVE v2010.4_26.16 : DRC_RES.db

File View Highlight Tools Window Setup Help

Topcell CHIP, 7 Results (in 7 of 324 Checks)

| Cell / Check | Results |
|----------------------|---------|
| ✓ Check M5.E.1 | 0 |
| ✓ Check M5.E.2 | 0 |
| ✓ Check M5.A.1 | 0 |
| ✓ Check VIA5.W.1 | 0 |
| ✓ Check VIA5.S.1 | 0 |
| ✓ Check VIA5.E.1 | 0 |
| ✓ Check VIA5.E.2 | 0 |
| ✗ Check PO.R.3 | 1 |
| ✗ Check M1.R.1 | 1 |
| ✗ Check M2.R.1 | 1 |
| ✗ Check M3.R.1 | 1 |
| ✗ Check M4.R.1 | 1 |
| ✗ Check M5.R.1 | 1 |
| ✓ Check ADP.R.0A | 0 |
| ✓ Check ADP.R.0B | 0 |
| ✓ Check ADP.R.0C | 0 |
| ✓ Check ADP.S.1_VIA1 | 0 |
| ✓ Check ADP.S.1_VIA2 | 0 |

```
NW.W.1 { @ Minimum NWEL width < 0.86
  INT NWEL < 0.86 ABUT < 90 SINGULAR REGION
}
```

Check NW.W.1, 0 Cells: 0 Results

Layout Versus Schematic



```
lvls.rep (~/.IC/ICC/verify/lvs) - gedit
檔案(E) 編輯(E) 顯示(V) 搜尋(S) 工具(T) 文件(D) 求助(H)
新增 開啓 儲存 列印... 復原 取消復原 剪下 複製 貼上 尋找 取代
CHIP_route.v x lvls.rep x
CELL COMPARISON RESULTS ( TOP LEVEL )
# # # # #
# # # CORRECT # #
# # # # #
# # # # #
#####
Warning: Ambiguity points were found and resolved arbitrarily.
Warning: LVS property resolution maximum exceeded.
LAYOUT CELL NAME: CHIP
SOURCE CELL NAME: CHIP
```


Queue Server



❖ Online DRC

CIC 工作站使用申請表(EPIC)

姓名:
學校: 國立勤益科技大學
系所: 電子所
指導教授: 林光浩
電話:
傳真:
E-Mail:

● 新增 Queue 帳號

製程名稱:
設計名稱:
連接到 Queue 的遠端主機:
連接到 Queue 的遠端帳號:

● 延長 Queue 帳號使用時間

Queue 伺服器帳號:
申請延長使用時間原因:

● 增加 Queue 帳號 Quota 大小

Queue 伺服器帳號:
增加 Quota 大小:
增加 Quota 原因:

```
#####
#
# 主旨:因應 Queue server系統微調作業, 暫停服務公告
#
#
# 因應Queue server設備系統微調作業, 預計時間為101/4/24(星期二)
#
# ~ 101/5/1(星期二), 屆時Queue Server對外服務將暫停。
#
#
# 造成不便, 敬請見諒!若有重要行程執行請避開上述停機時間!!!
#
#
# 系統管理員 101.4.24
#####
queue.cic.org.tw ~> ls
2.01_CHIP_ECC.gds
result_12-2-21_cicq78f_DRC_queue_9349
result_12-2-18_cicq78f_DRC_queue_2615
result_12-2-21_cicq78f_LPE_queue_9390
result_12-2-18_cicq78f_LPE_queue_2548
result_12-3-6_cicq78f_DRC_queue_4120
result_12-2-18_cicq78f_LPE_queue_2828
queue.cic.org.tw ~> Qentry -M DRC -tech TSMC18 -f 2.01_CHIP_ECC.gds -T CHIP -c T
SMC18 -i TSMC18 -addTagCell -addDummyCell
```

Taped-out via CIC



- ❖ Before Taped-out, make sure that
 - Your design is DRC clean.
 - Your design passes the block-box LVS check.
 - Your design meet the timing/power specification.
- ❖ When taped-out via CIC, prepare the following:
 - GDSII layout of your design
 - Calibre DRC report file
 - Calibre LVS report file
 - Post-layout timing/power verification result
 - Specification files of used memories



下線準備資料



❖ 下線所需要上傳的資料有下列五種：

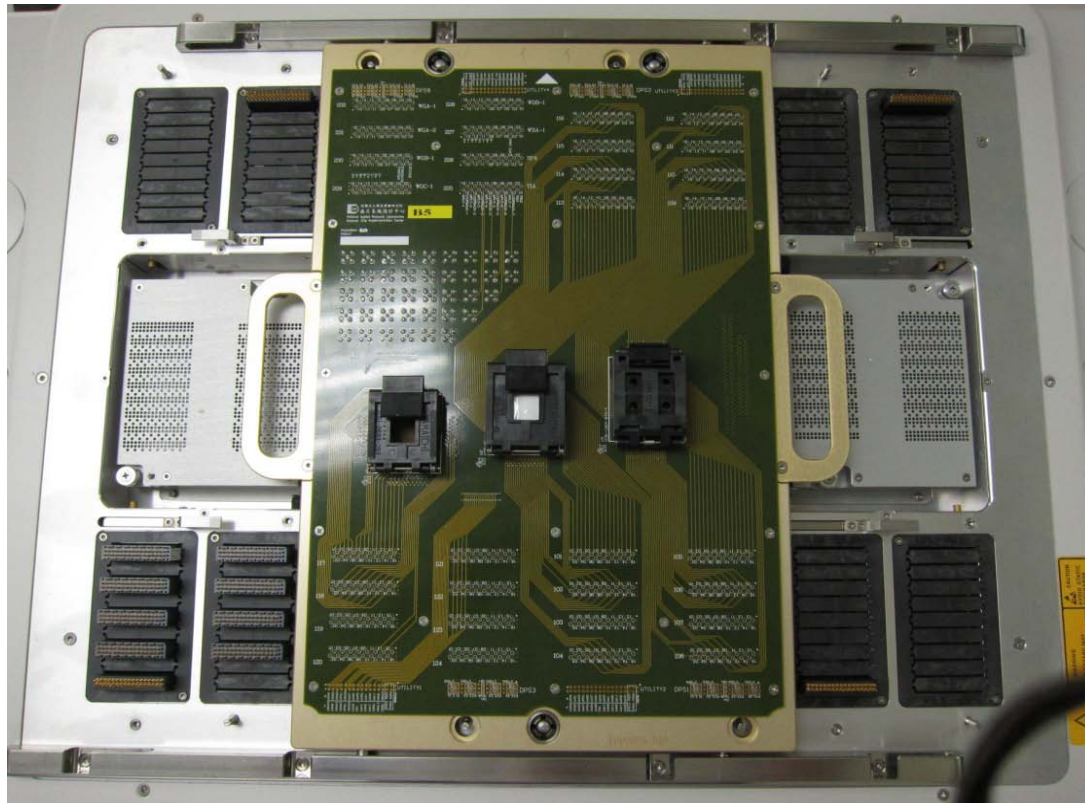
- 1. 下線報告(Word)
- 2. layout完成的gds檔
- 3. DRC.rep(看DRC錯誤的檔案)
- 4. lvs.rep(有笑臉的檔案)
- 5. tapeout報告(Word, 附件二)

❖ 需準備的檔案有下列兩種：

- 1. 檔名:上傳號碼；內容:學校信箱
- 2. ok檔；內容:ok

❖ 上傳方式請參考附件三。

Automatic Test System

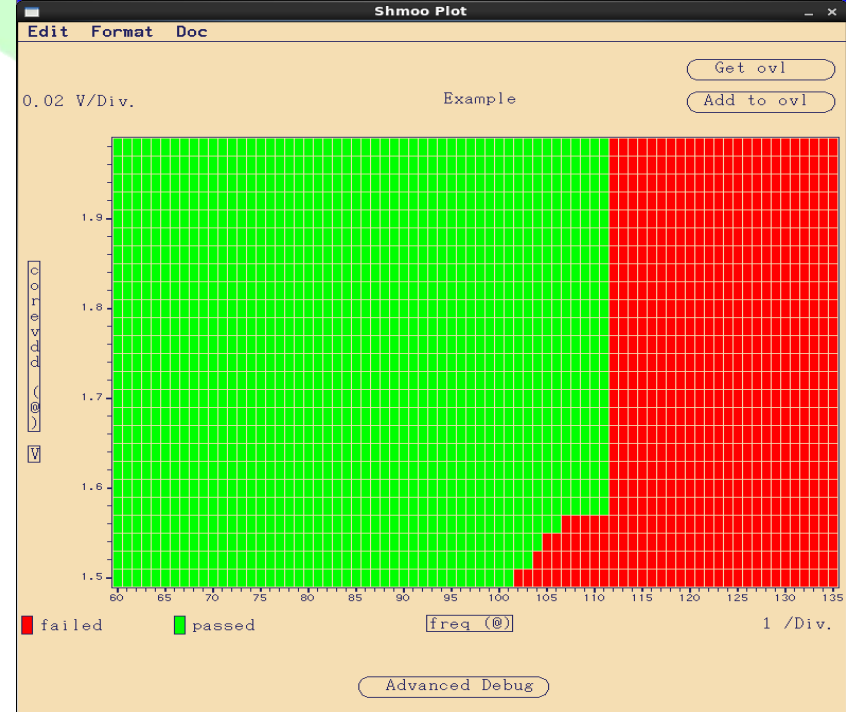
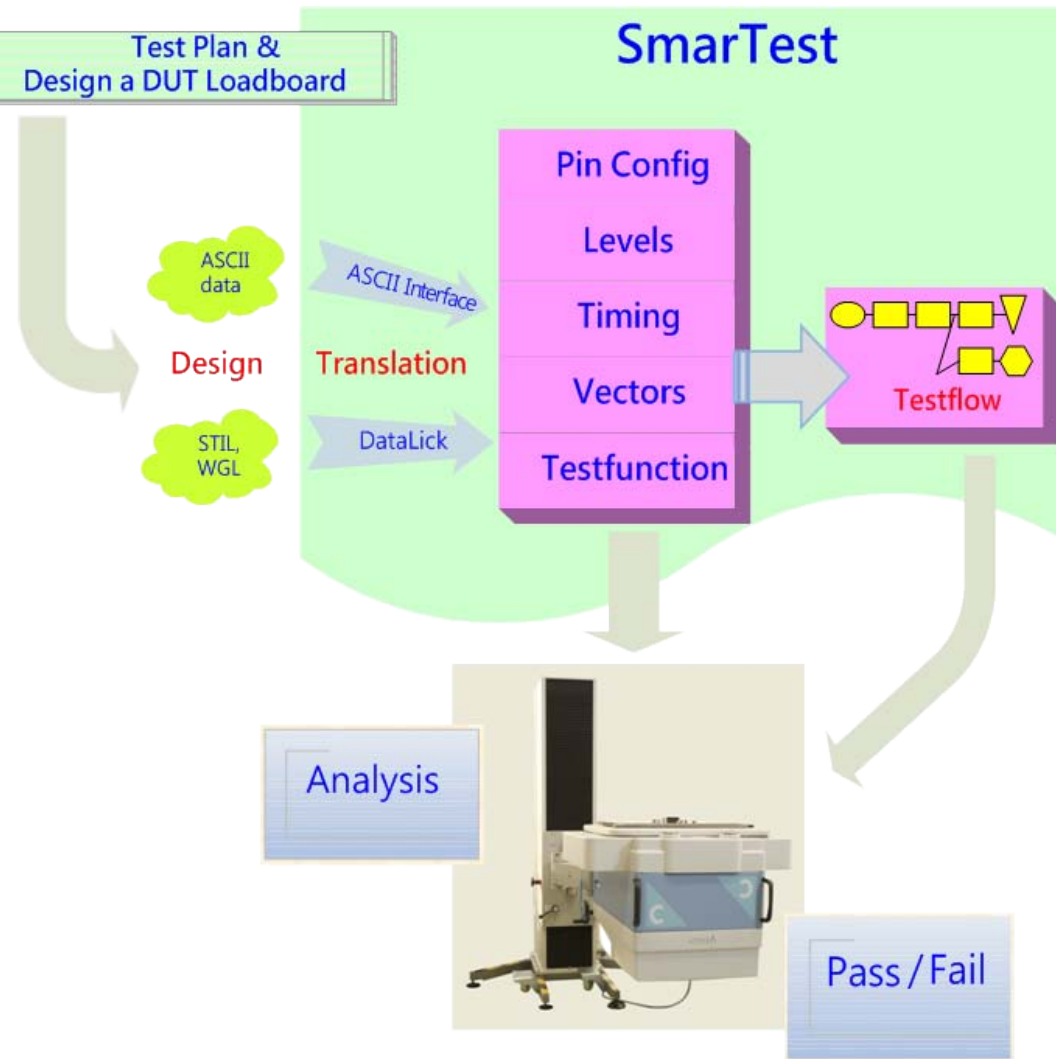


ADVANTEST V93000 PS1600
CIC Package : CQFP, LCC, SB

Ref : NAR Labs 國家晶片系統設計中心



Automatic Test System (Cont.)



Ref : NAR Labs 國家晶片系統設計中心

Programmable Logic

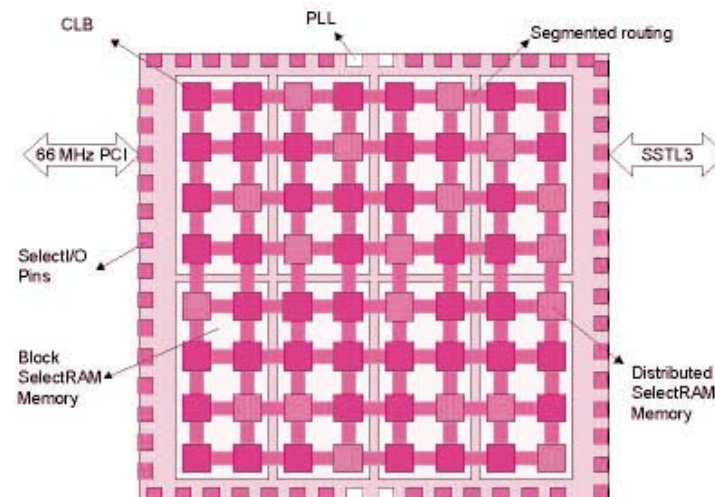


- ❖ PLD (Programmable Logic Device) according to their structure and density can be divided into three categories
 - SPLD (Simple Programmable Logic Device)
 - CPLD (Complex Programmable Logic Device)
 - FPGA (Field Programmable Gate Array)

❖ Xilinx

❖ Altera

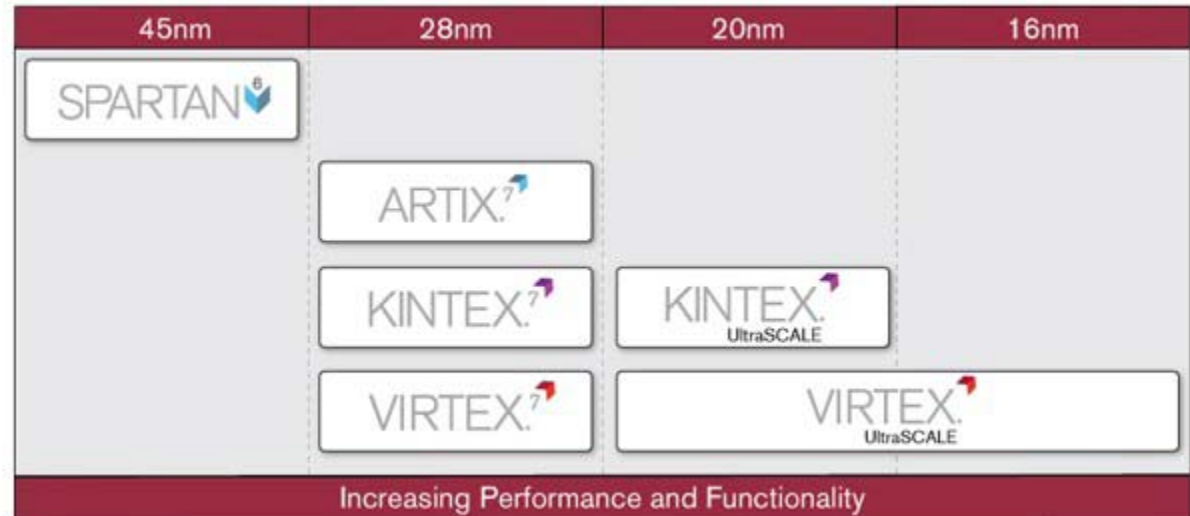
❖ Actel (Microsemi)

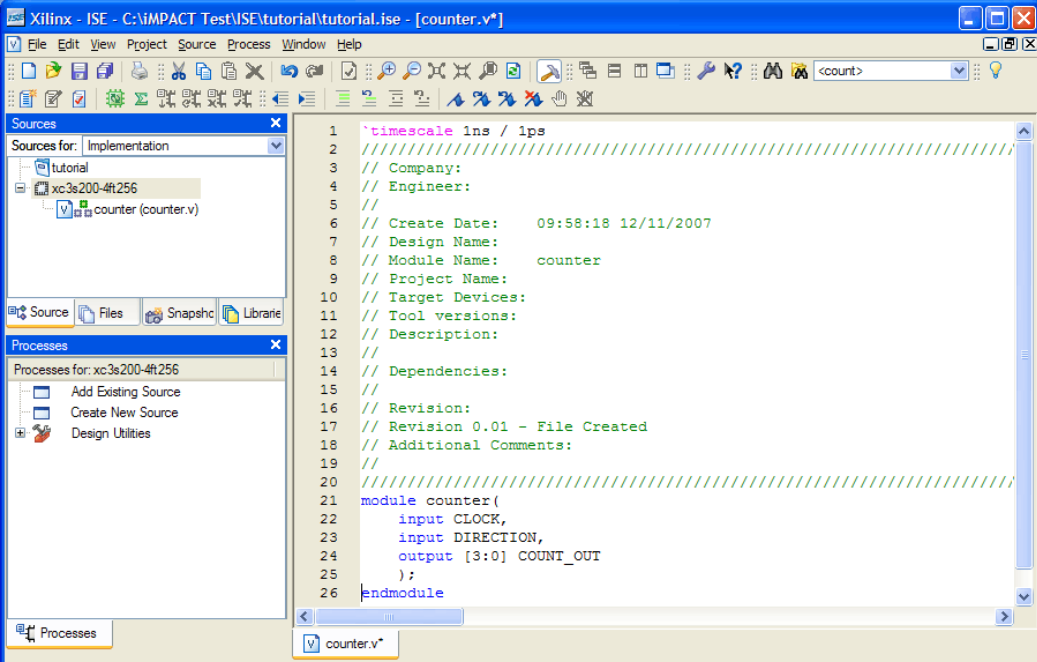


Xilinx



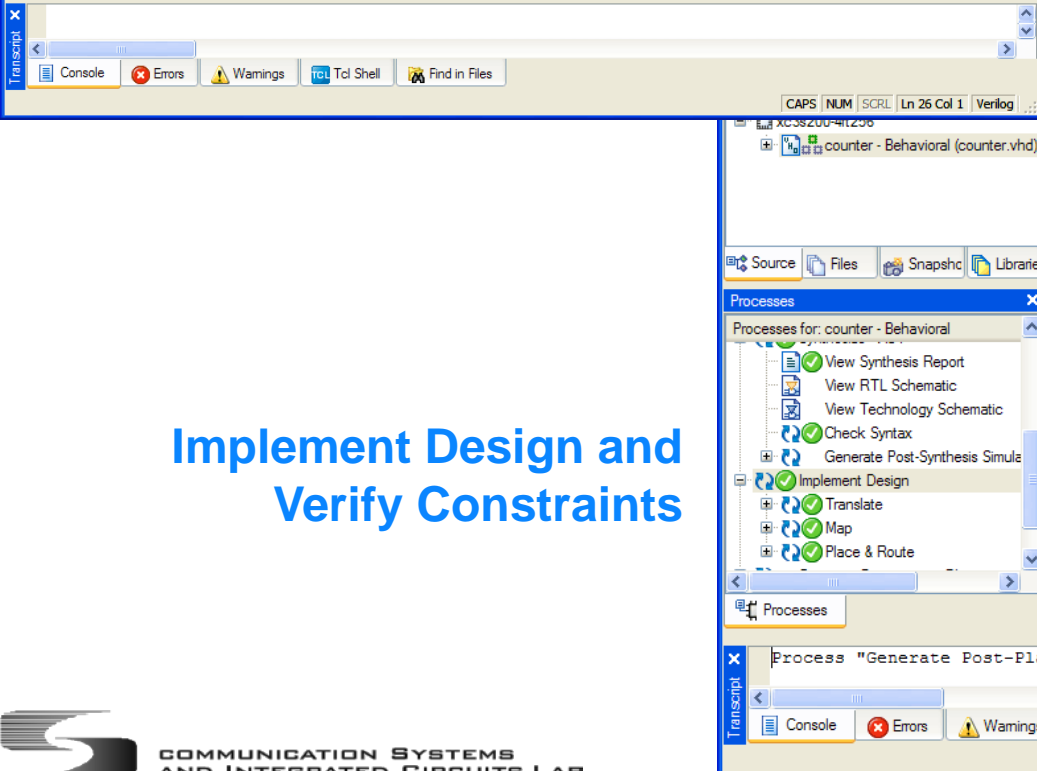
| | Spartan-6 | Artix-7 | Kintex-7 | Virtex-7 |
|--|---------------------------|-------------------------|--------------------------|--------------------------|
| Logic Cells | 150,000 | 215,000 | 480,000 | 2,000,000 |
| BlockRAM | 4.8Mb | 13Mb | 34Mb | 68Mb |
| DSP Slices | 180 | 740 | 1,920 | 3,600 |
| DSP Performance (symmetric FIR) | 140GMACs | 930GMACs | 2,845GMACs | 5,335GMACs |
| Transceiver Count | 8 | 16 | 32 | 96 |
| Transceiver Speed | 3.2Gb/s | 6.6Gb/s | 12.5Gb/s | 28.05Gb/s |
| Total Transceiver Bandwidth (full duplex) | 50Gb/s | 211Gb/s | 800Gb/s | 2,784Gb/s |
| Memory Interface (DDR3) | 800Mb/s | 1,066Mb/s | 1,866Mb/s | 1,866Mb/s |
| PCI Express® Interface | x1 Gen1 | x4 Gen2 | x8 Gen2 | x8 Gen3 |
| Analog Mixed Signal (AMS)/XADC | | Yes | Yes | Yes |
| Configuration AES | Yes | Yes | Yes | Yes |
| I/O Pins | 576 | 500 | 500 | 1,200 |



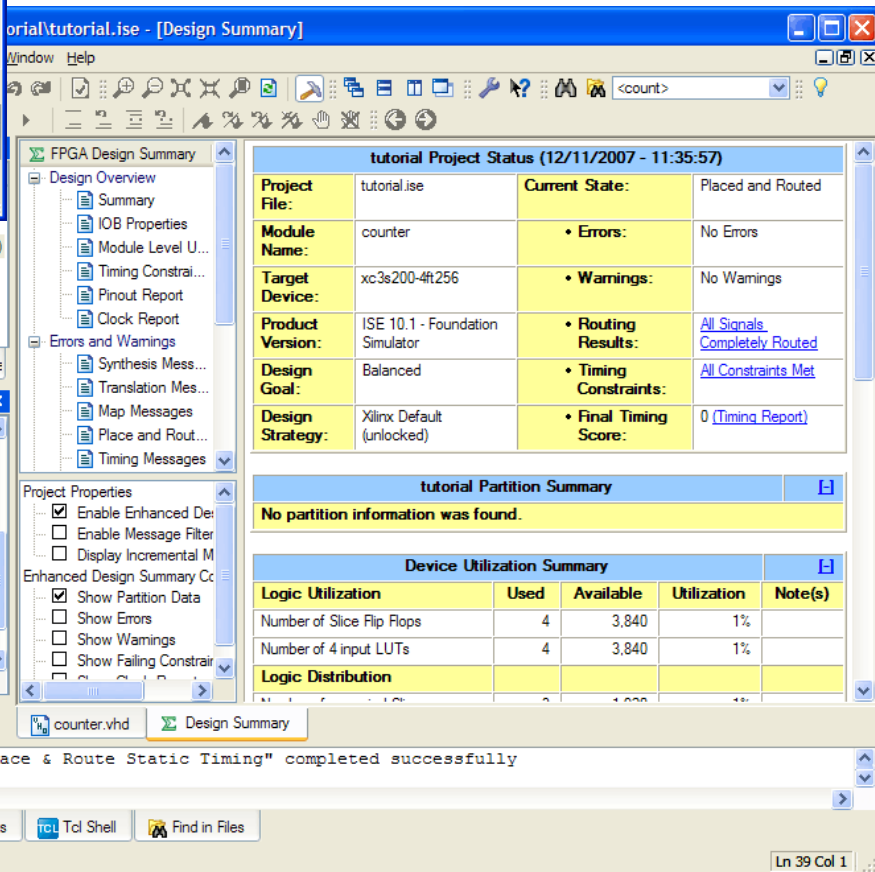


Xilinx ISE

Create an HDL Source



Implement Design and Verify Constraints



Xilinx PACE - C:\tutorial\counter.ucf

File Edit View IOBs Areas Tools Window Help

Design Browser

- I/O Pins
- Global Logic
- Logic

Design Object List - I/O P...

| I/O Name | I/O Direction | Loc | Ba |
|--------------|---------------|-----|----|
| CLOCK | Input | i9 | BA |
| COUNT_OUT<0> | Output | k12 | BA |
| COUNT_OUT<1> | Output | p14 | BA |
| COUNT_OUT<2> | Output | i12 | BA |
| COUNT_OUT<3> | Output | n14 | BA |
| DIRECTION | Input | k13 | BA |

Package Pins for xc3s200-4-ft256

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

A
C
E
F
G
H
J
K
L
M
N
P
F
T

Package View Architecture V

Xilinx ISE (Cont.)



Assigning Pin Location Constraints

Download Design to the Demo Board

Desktop Configuration
Direct SPI Configuration
SystemACE
PROM File Formatter

Sources Snapshots Libraries Configuration Modes

Processes

Processes Configuration Operations

Transcript

```
// *** BATCH CMD : setMode -bs
// *** BATCH CMD : setMode -bs
GUI --- Auto connect to cable...
// *** BATCH CMD : setCable -port auto
```

Console Errors Warnings Tcl Shell Find in Files

tutorial/tutorial.ise - [Boundary Scan]

Operations Output Debug Window Help

Diagram showing TDI and TDO connections to xc3s200 and xc3s200 devices.

Assign New Configuration File

Look in: C:\Projects\jade\QST\tutorial\

- isim
- isim.tmp_save
- netgen
- templates
- xst
- counter.bit

File name: _____ Open

File type: All Design Files (*.bit *.rpt *.nky *.isc *.bsd) Cancel

None

- Enable Programming of SPI Flash Device Attached to this FPGA
- Enable Programming of BPI Flash Device Attached to this FPGA

Design Summary Boundary Scan

Configuration Parallel III 200 KHz LPT1

Altera



High-End FPGAs



- Highest bandwidth, highest density FPGAs
- Integrated transceiver variants
- Design entire systems on a chip

Midrange FPGAs

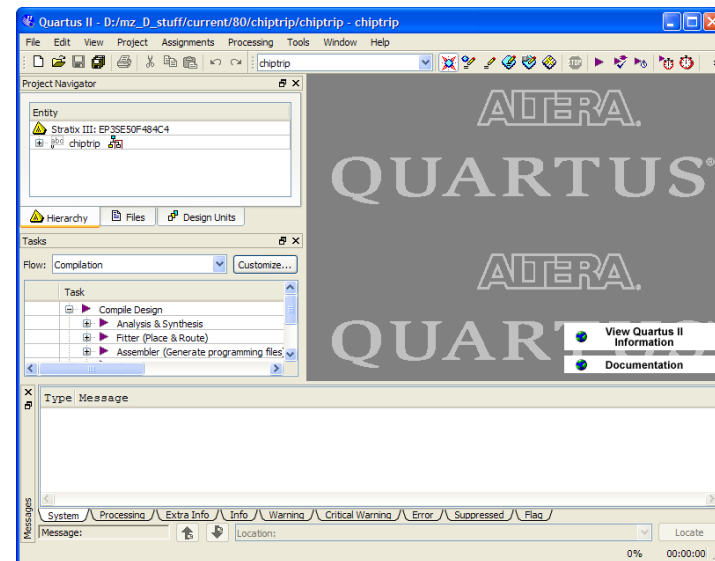
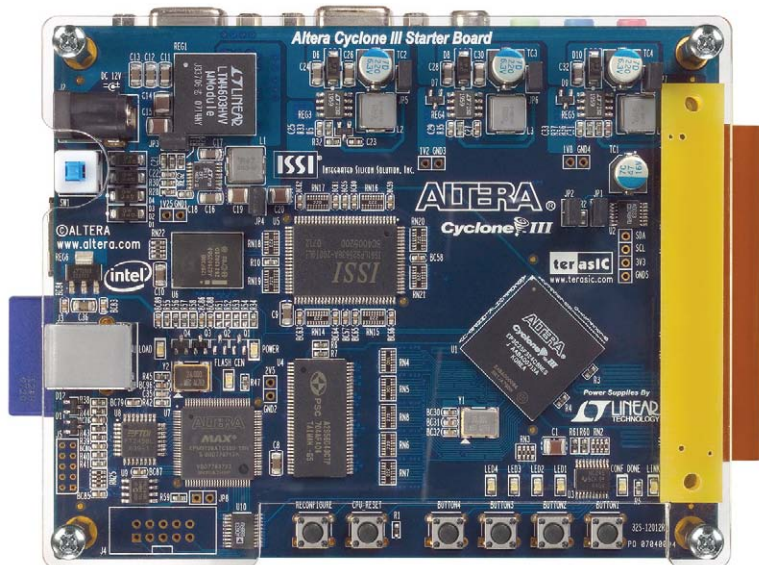


- Balanced cost, power, and performance FPGAs
- Integrated transceiver and processor variants
- Comprehensive design protection

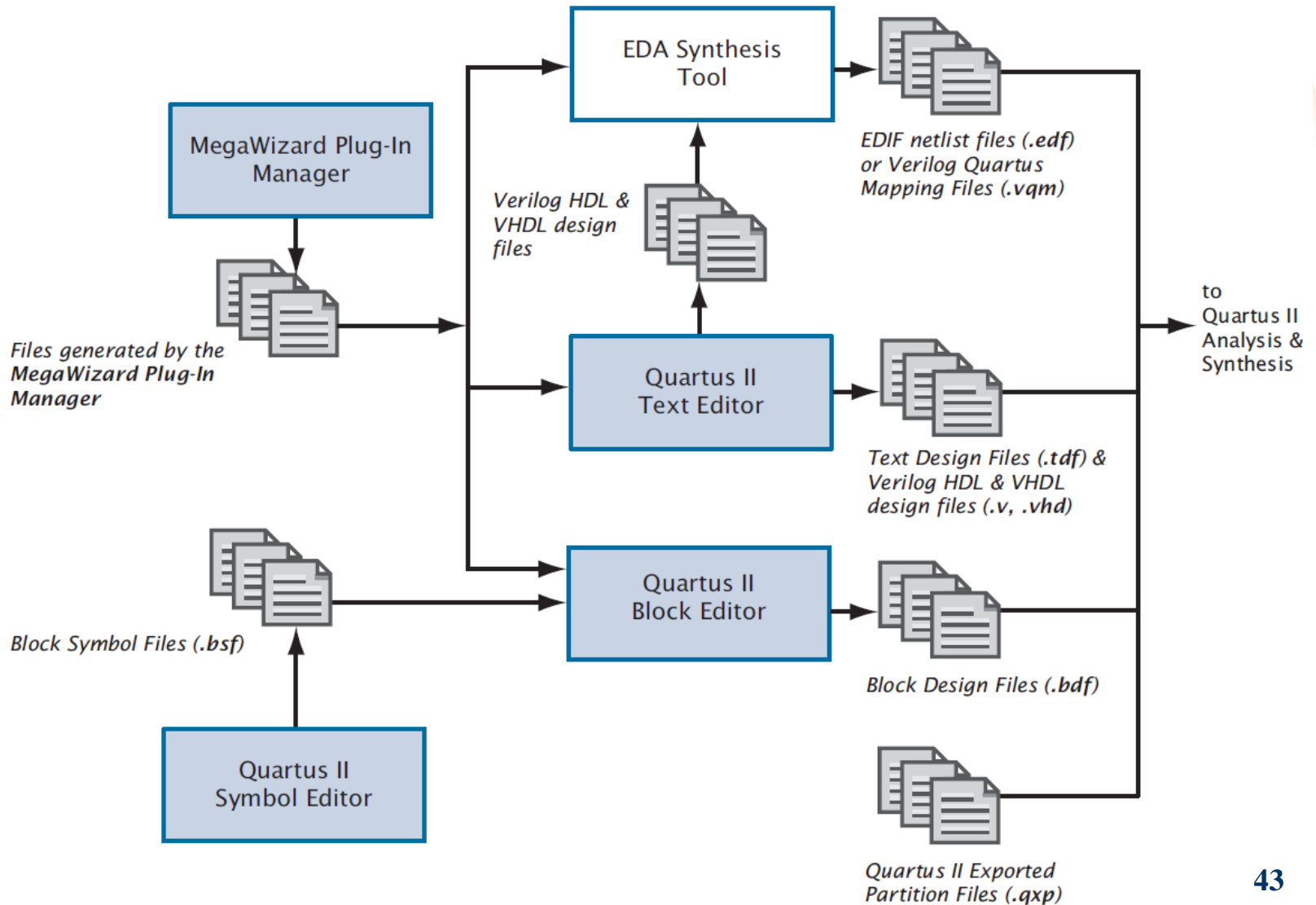
Lowest Cost and Power FPGAs

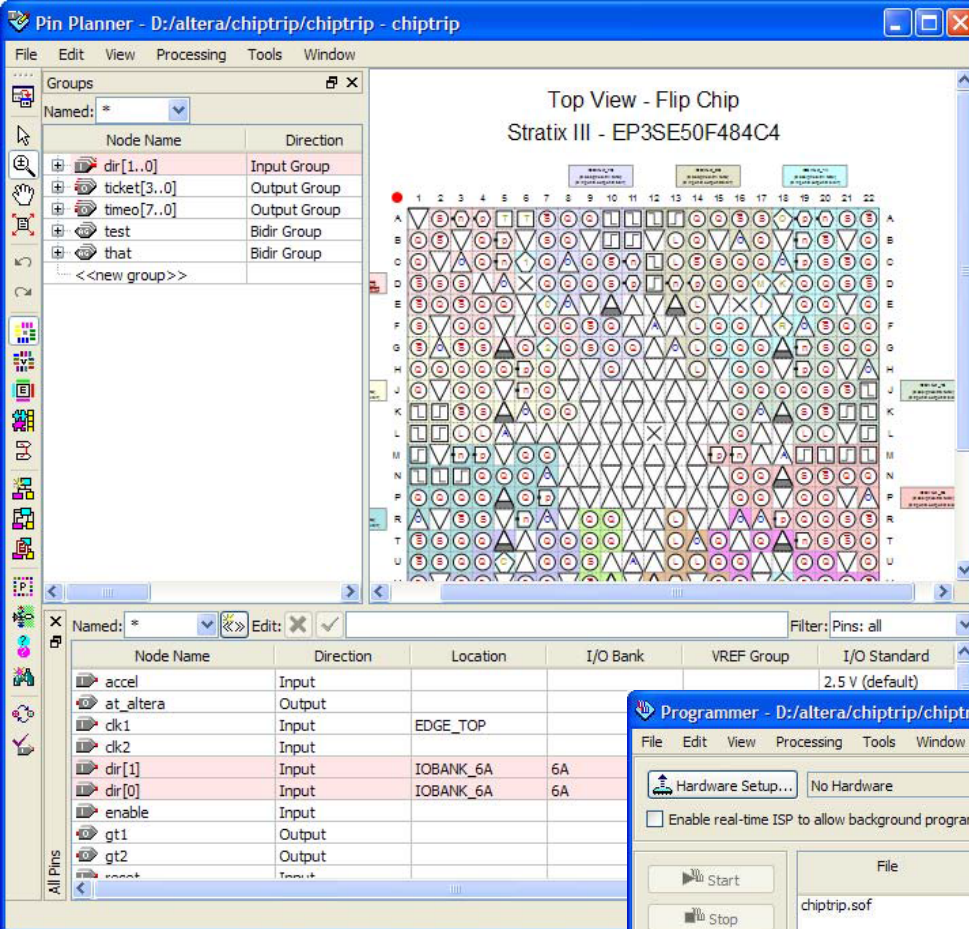


- Lowest system cost and power FPGAs
- Integrated transceiver and processor variants
- Fastest time to market



QUARTUS II Design Entry Flow



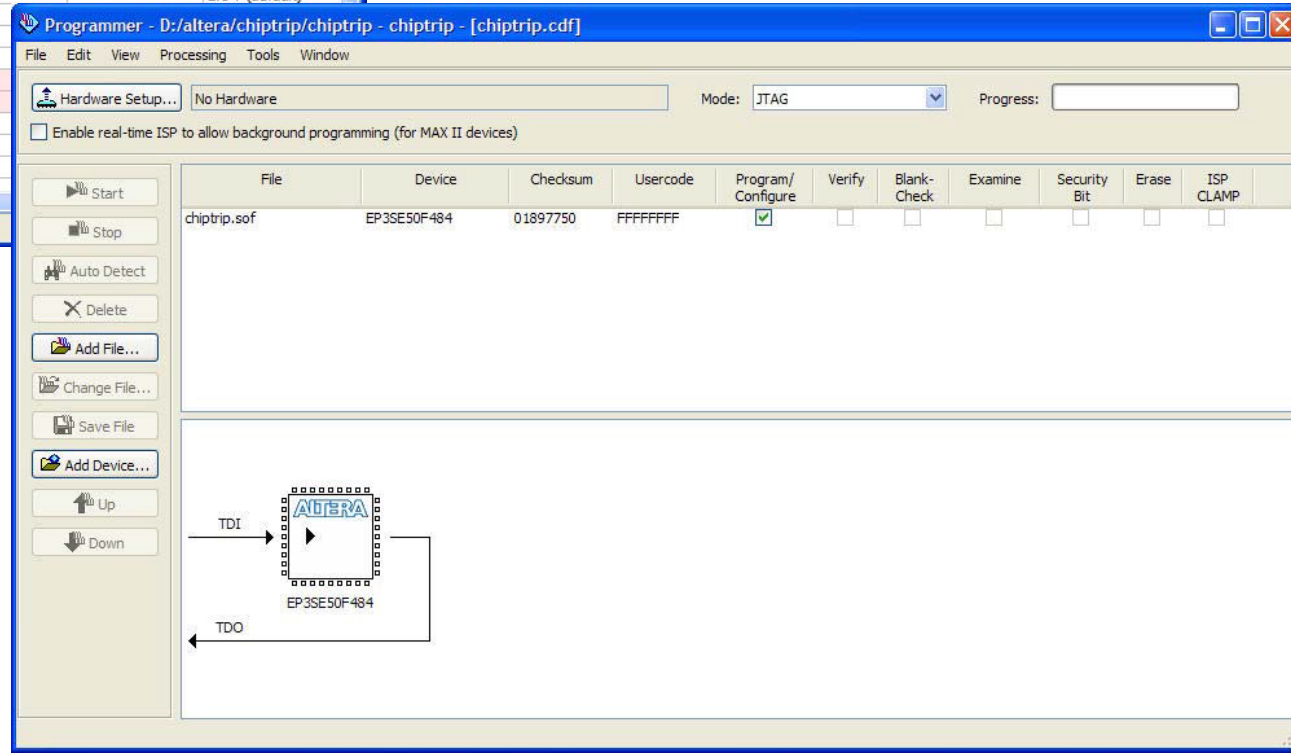


QUARTUS II

Pin Planner



Programmer

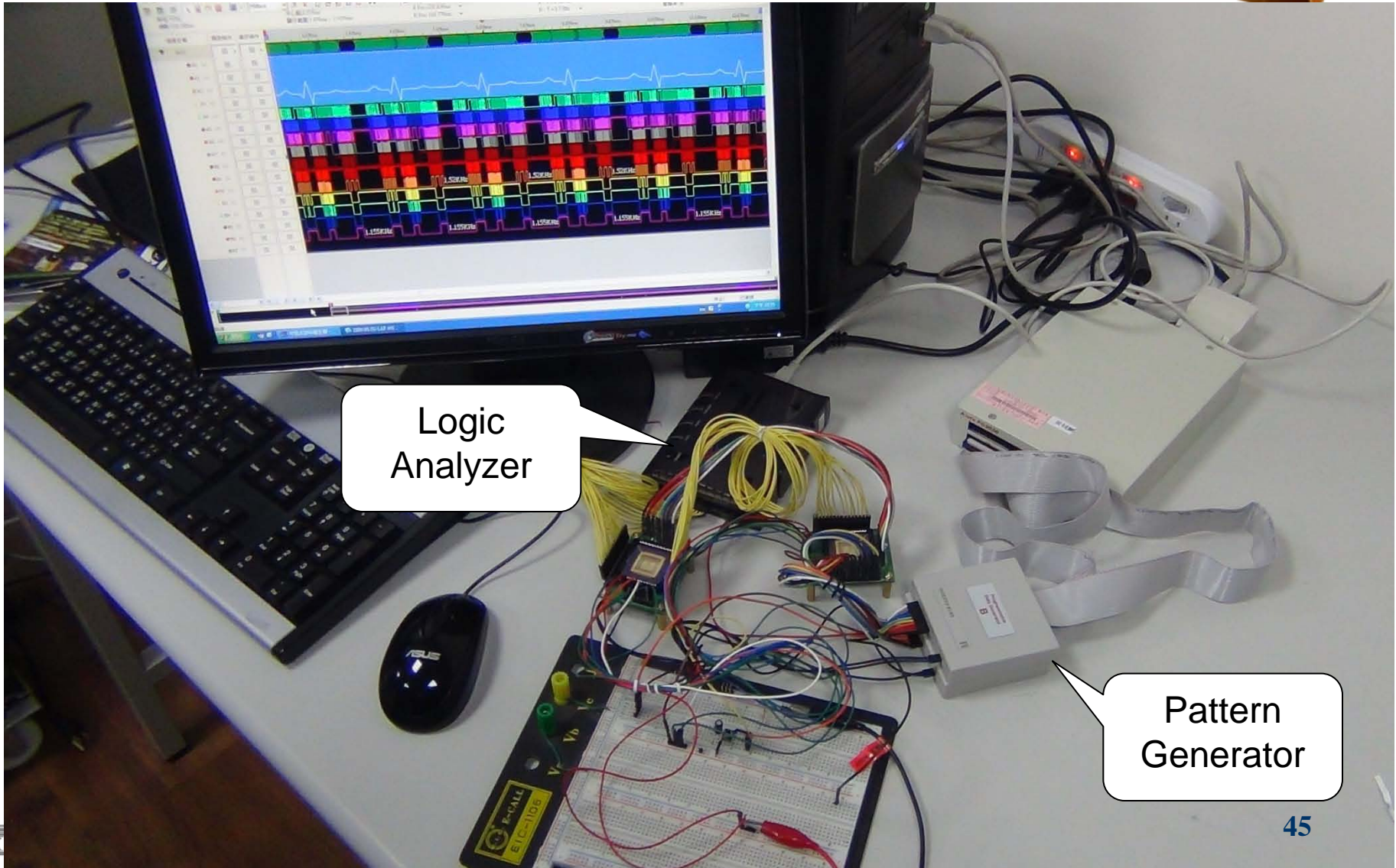


QUARTUS® II



COMMUNICATION SYSTEMS
AND INTEGRATED CIRCUITS LAB

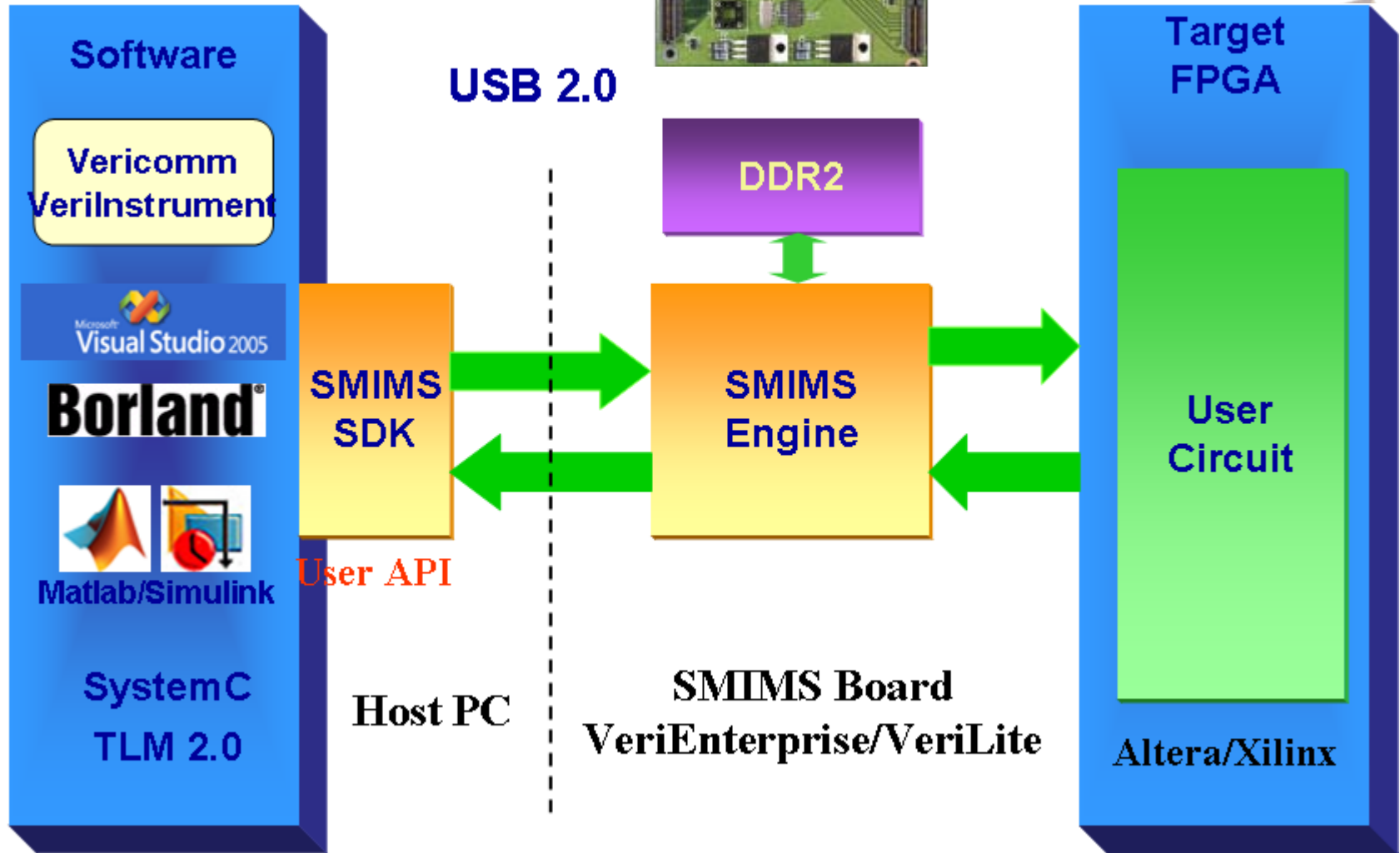
Measurement



Logic Analyzer

Pattern Generator

SMIMS



Outline



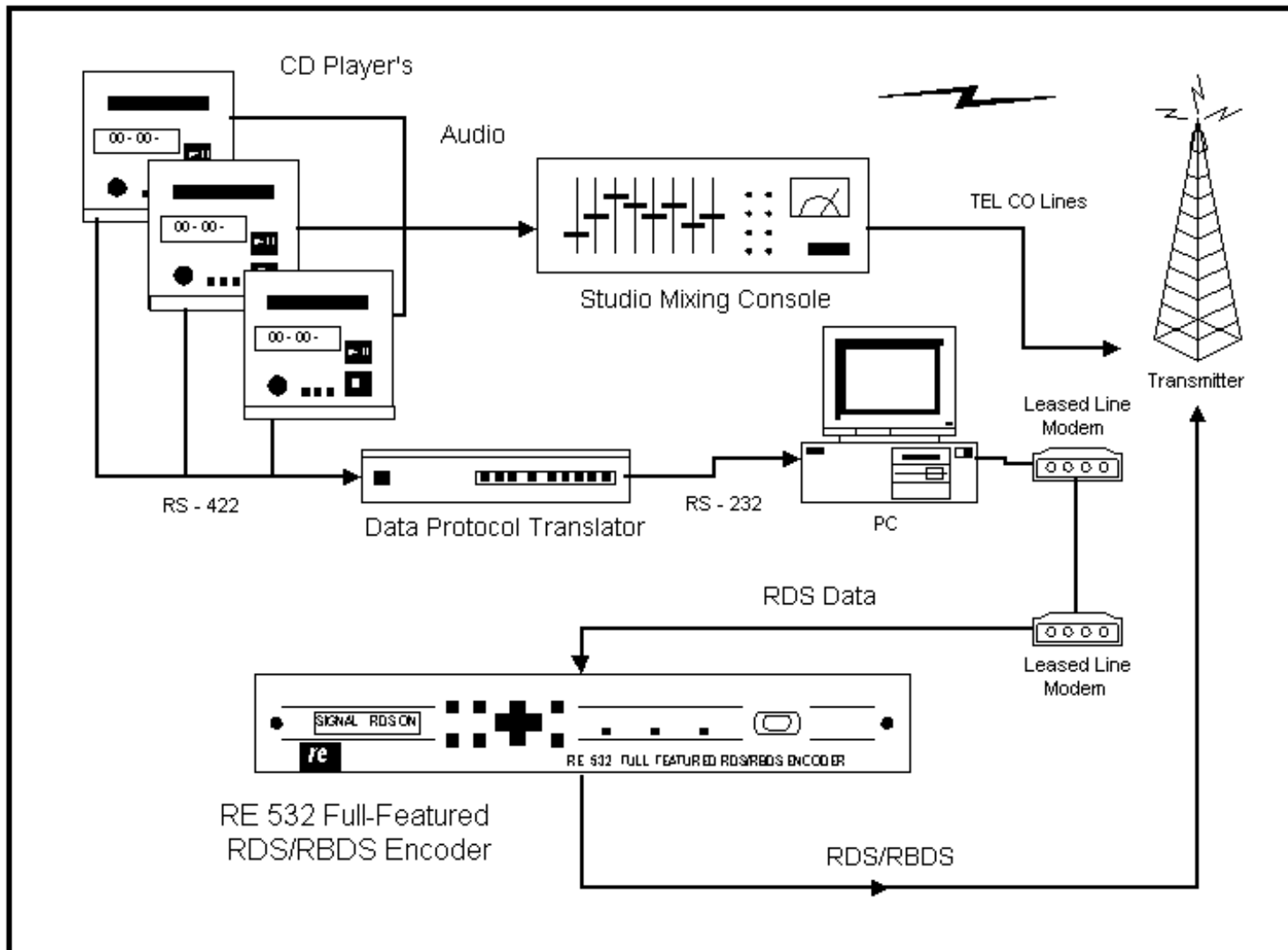
- 1 Integrated Circuit
- 2 Chip Design
- 3 Application

System Application

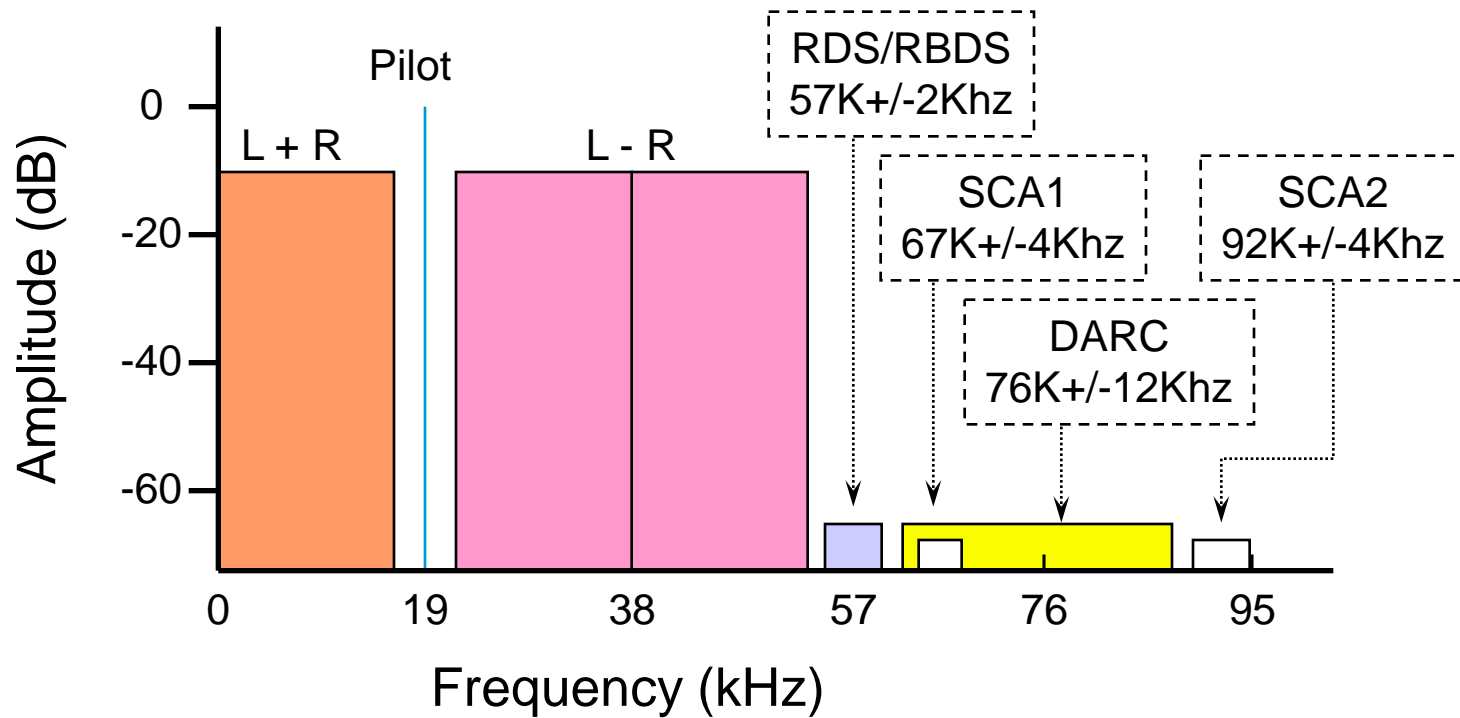


- ❖ Radio Data System
- ❖ 智慧電子國家型科技計畫(NPIE) -- Interactive Intelligent Healthcare System
- ❖ PCB board Circuits Design
- ❖ IC Samples

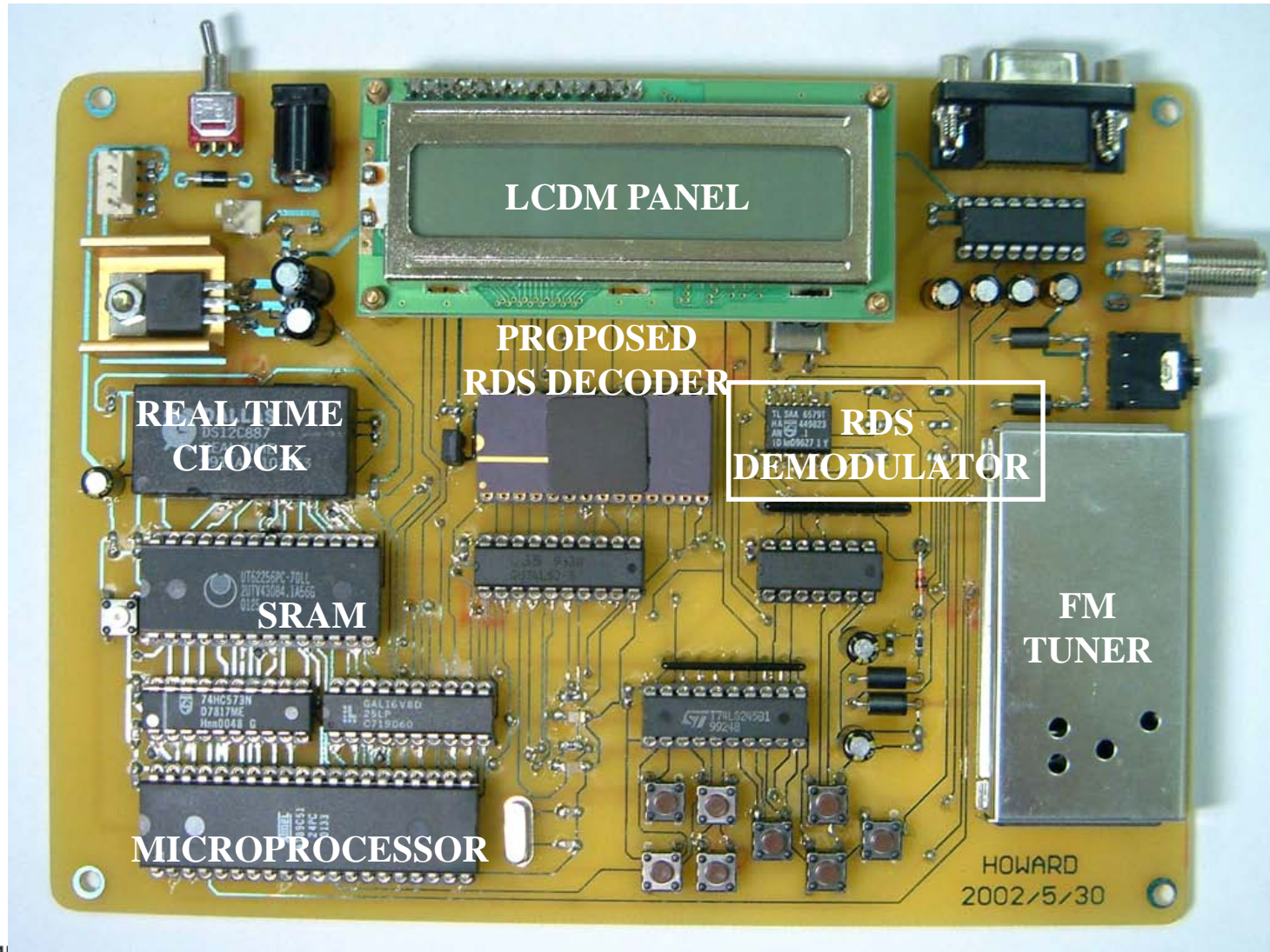
Digital RDS Demodulation in FM Subcarrier Systems



Radio Data System



RDS Receiver Physical Circuit



LCDM PANEL

PROPOSED
RDS DECODER

RDS
DEMODULATOR

REAL TIME
CLOCK

SRAM

FM
TUNER

MICROPROCESSOR

HOWARD
2002/5/30

Measurement Environment



RDS DECODER RDS Receiver

Healthcare Monitoring

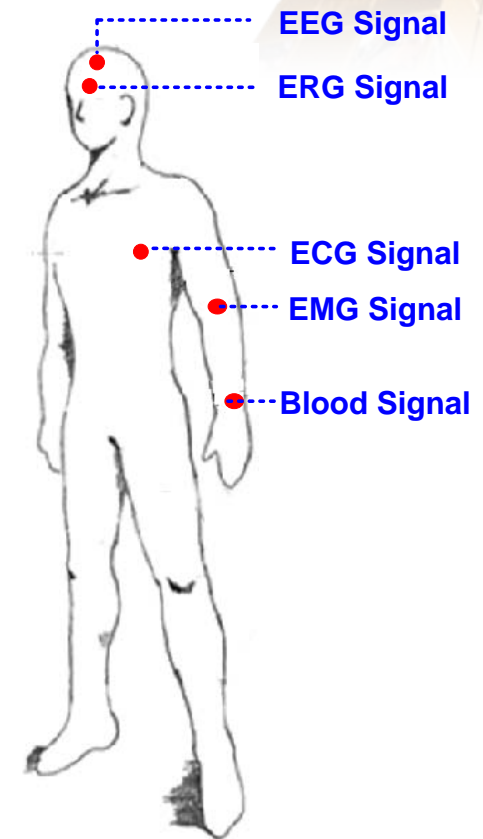


◆ Motivation

- ◆ Aging Population, Intensity lifestyle
 - ◆ Pressure, Nervousness, Disturbance
 - ◆ Chronic Cardiovascular Diseases
- ◆ Bio-microsystem application
 - ◆ EEG, ERG, ECG, EMG, Blood.

◆ Intelligent Healthcare Monitoring

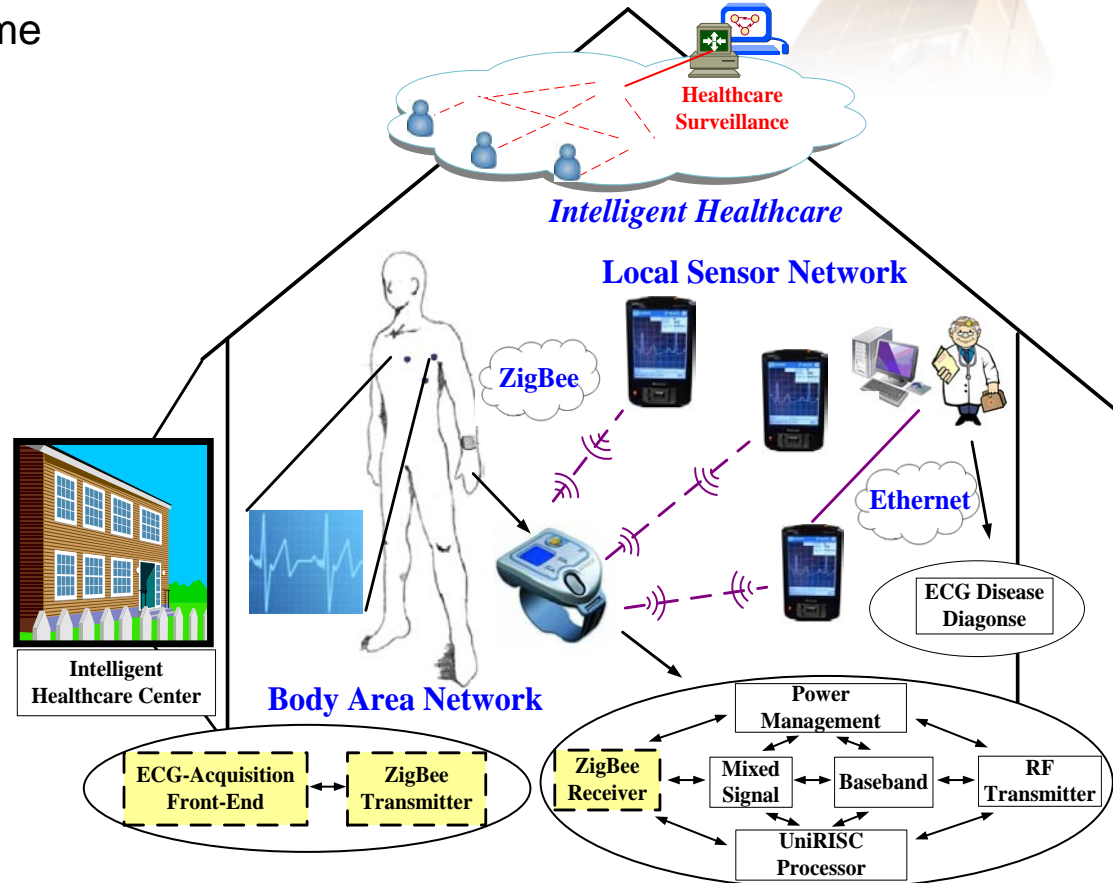
- ◆ Interactive, Low Power, Wireless SoC
 - ◆ IEEE 802.15.4 ZigBee Application
 - ◆ 2.4GHz ISM Band



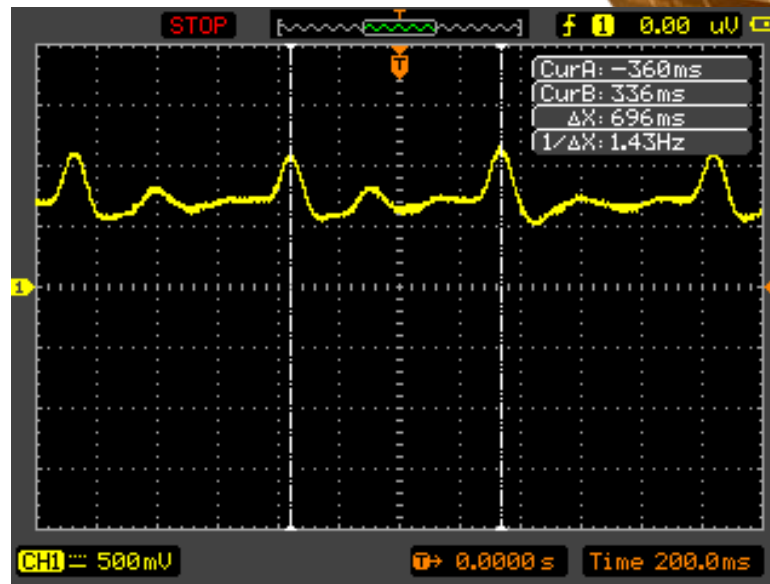
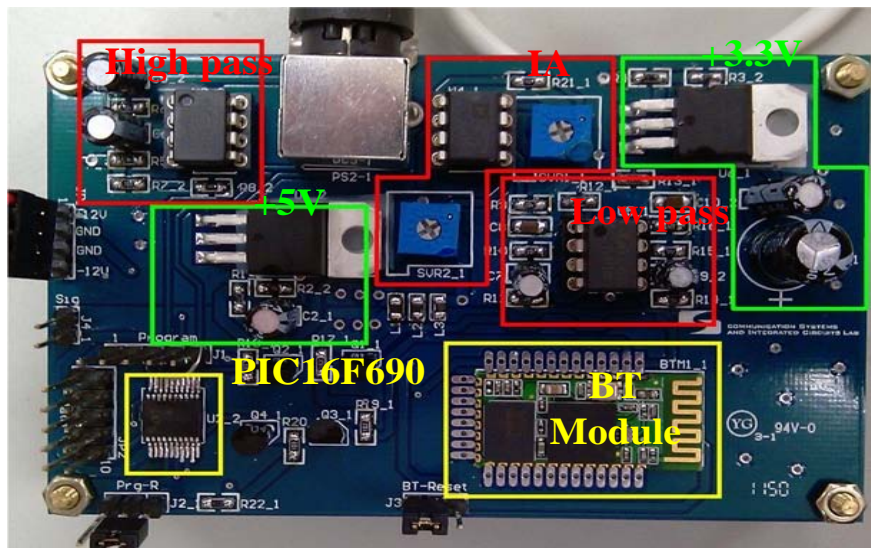
Interactive Intelligent Healthcare System



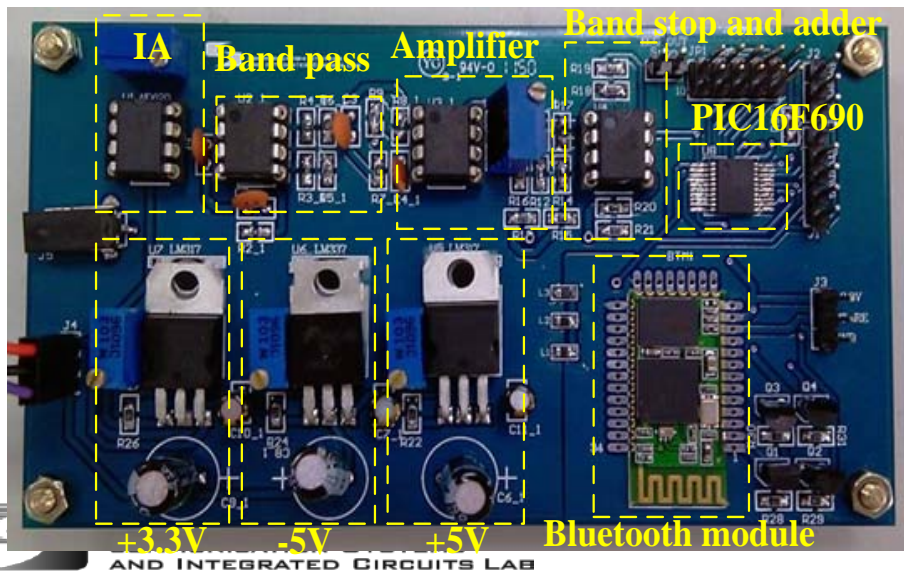
- Targets
 - Low Power, Anywhere, Anytime
 - Long-term Monitoring
- Body Area Network
 - Near-Body Application
 - Acquisition Node
 - Wearable Device (watch)
- Local Sensor Network
 - Intermediate Interface
 - Wearable Device
 - Portable Facility (PDA)



SpO₂ & ECG Circuits Design

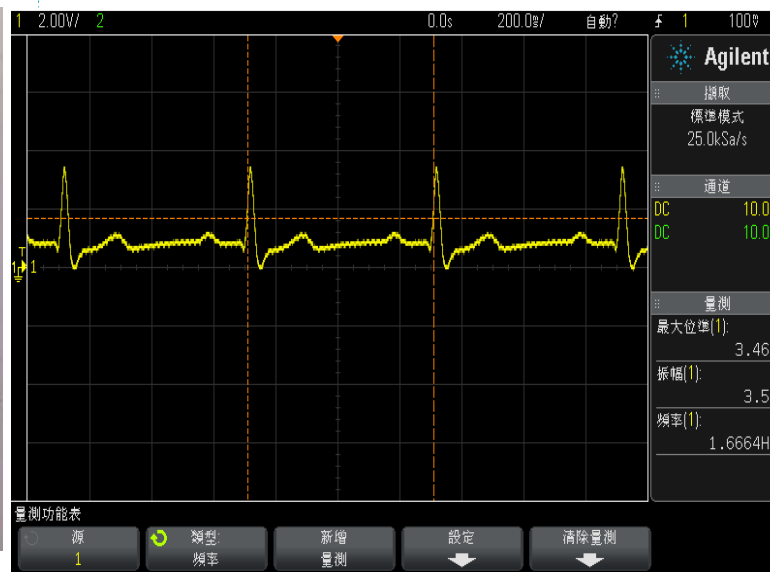


SpO₂



Agilent Technologies

Mon Dec 26 15:29:41 2011

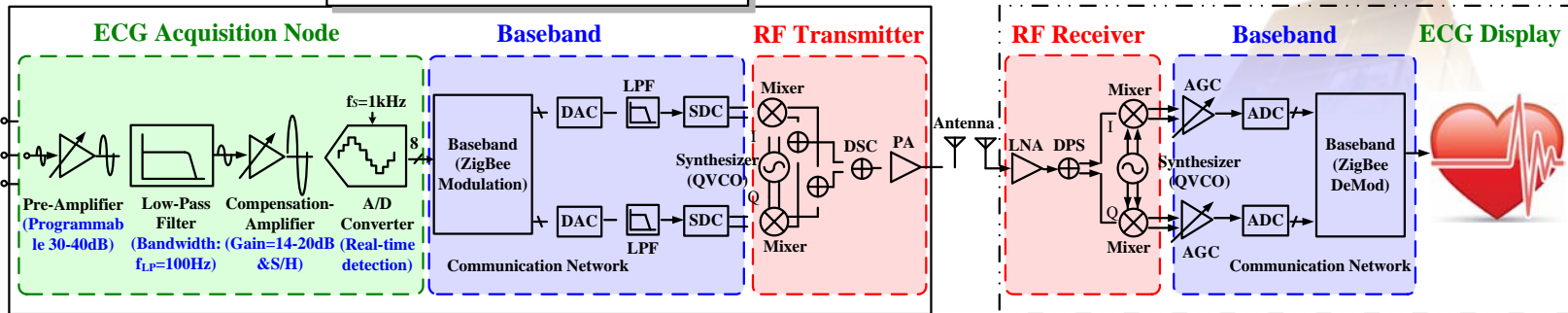


ECG

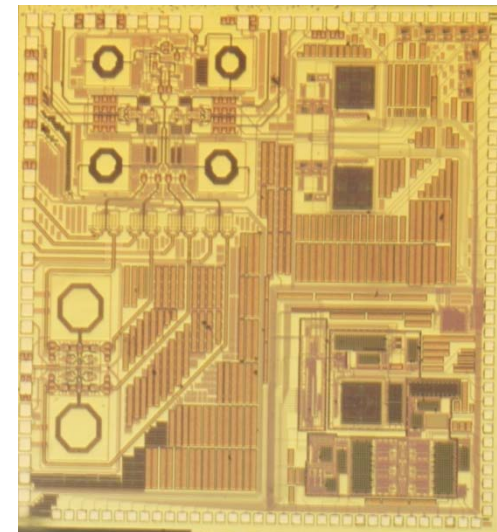
System Block Diagram



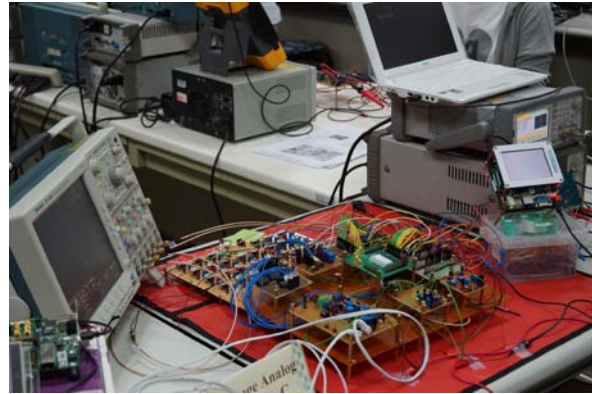
Wireless Bio-Signal Acquisition SoC



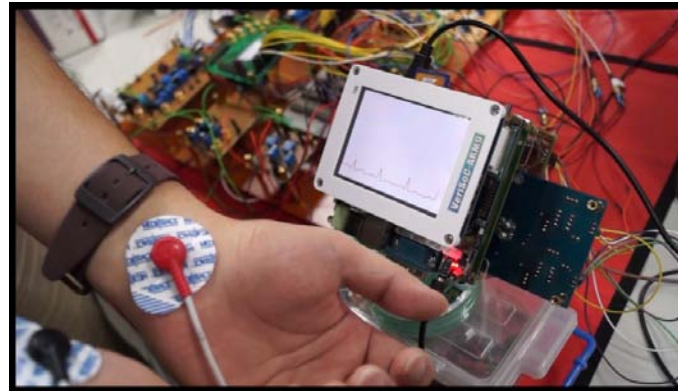
- Transmitter : Wireless Bio-Signal Acquisition SoC (WBSA-SoC)
 - AFE : PreAmp., Filter, PostAmp., 8-bit SAADC
 - Baseband : ZigBee Spread Spectrum Technology
 - RF Front-end : VCO, Up-Mixer, PA
- Receiver: ARM Display
 - RF Front-end : LNA, Down-Mixer
 - Mixed-Mode Board: BPF, AGC, ADC
 - Based-Band & Display : ZigBee Demod. & ARM-base Display



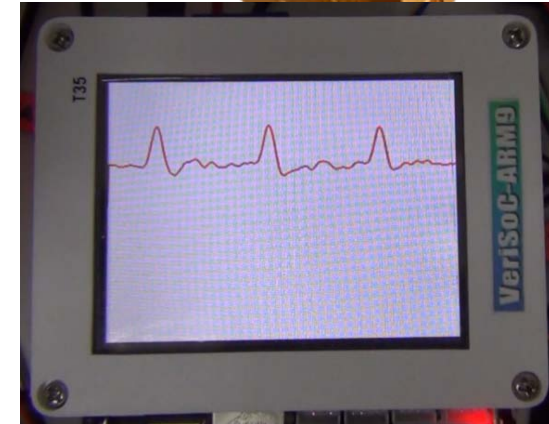
System Experiment Result



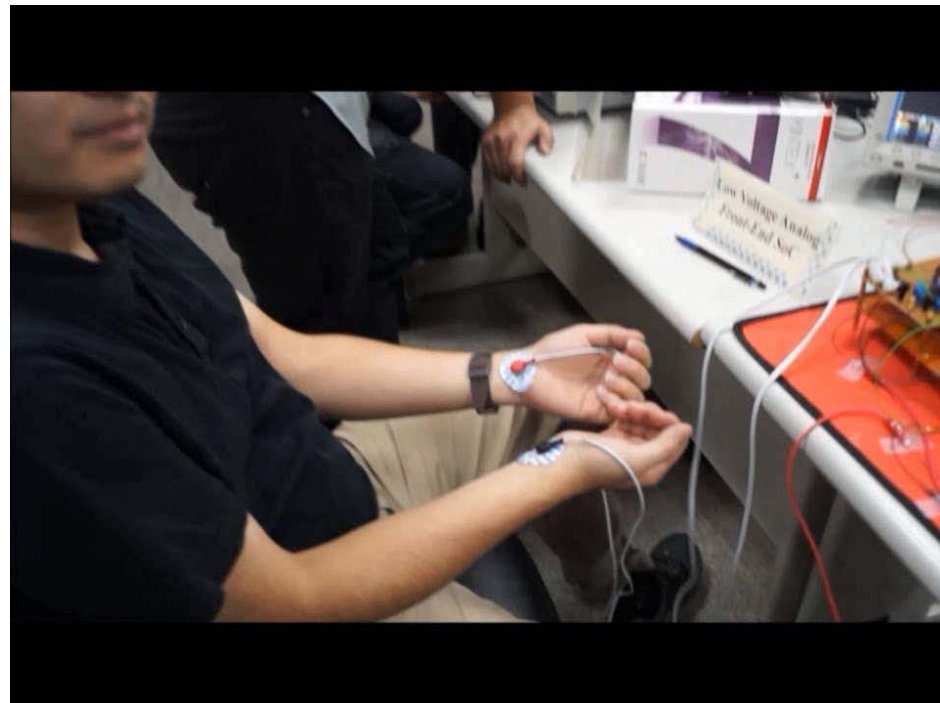
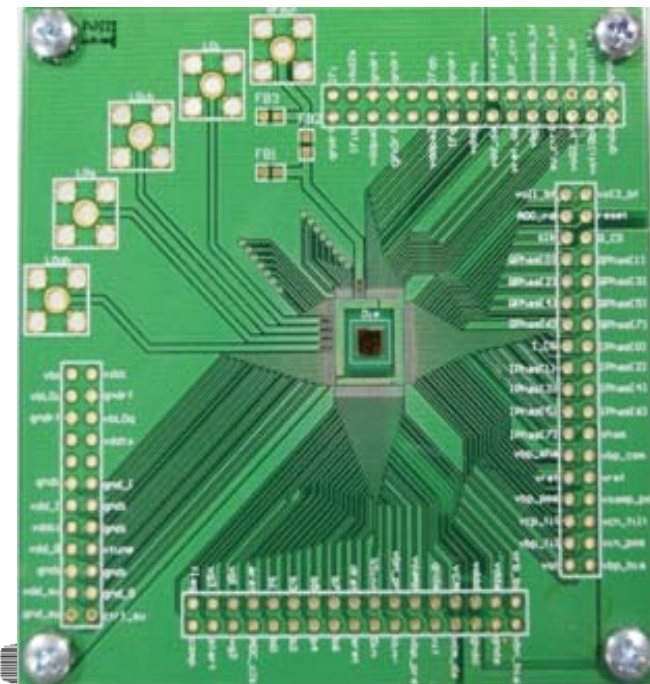
Verification Setup



Measurement Setup

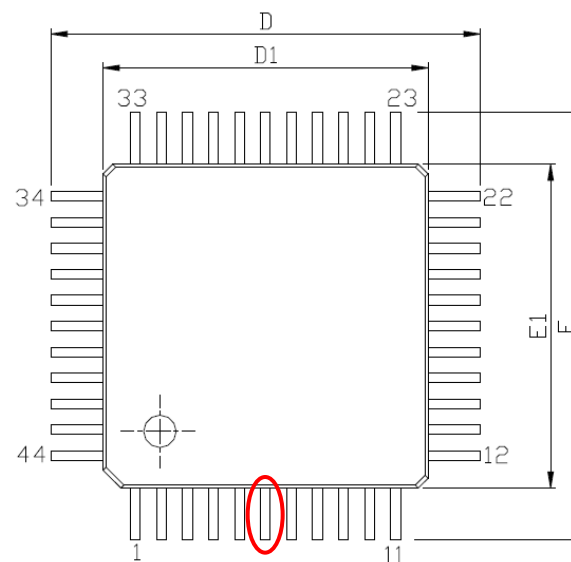
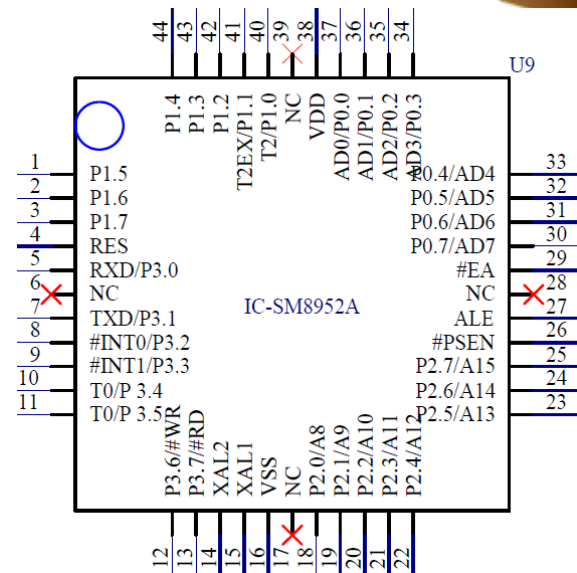
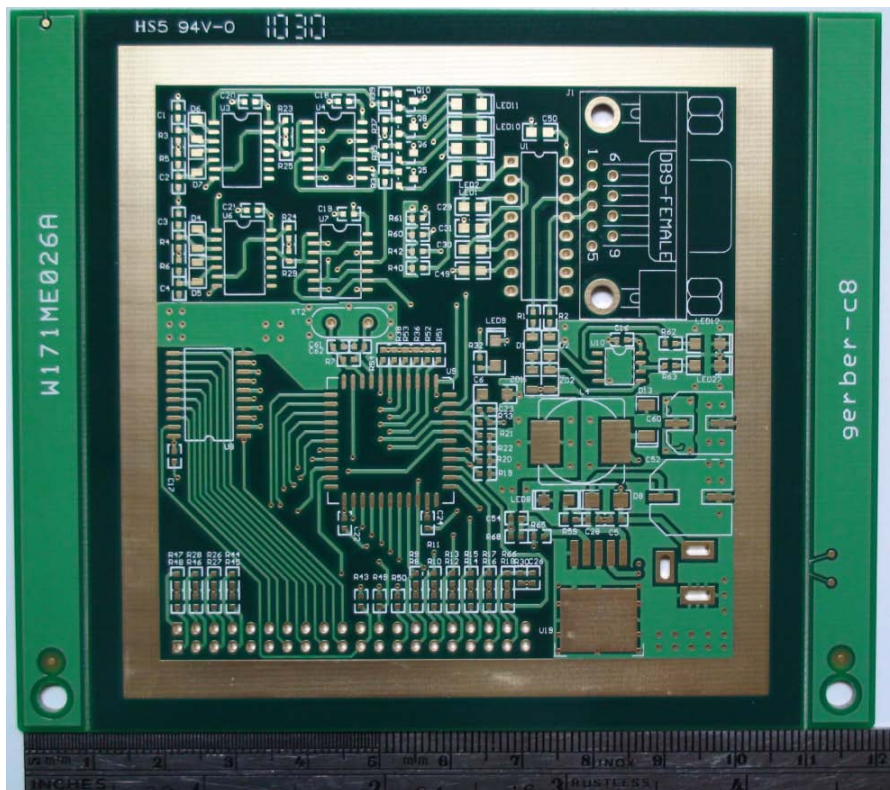


Display with ARM Platform

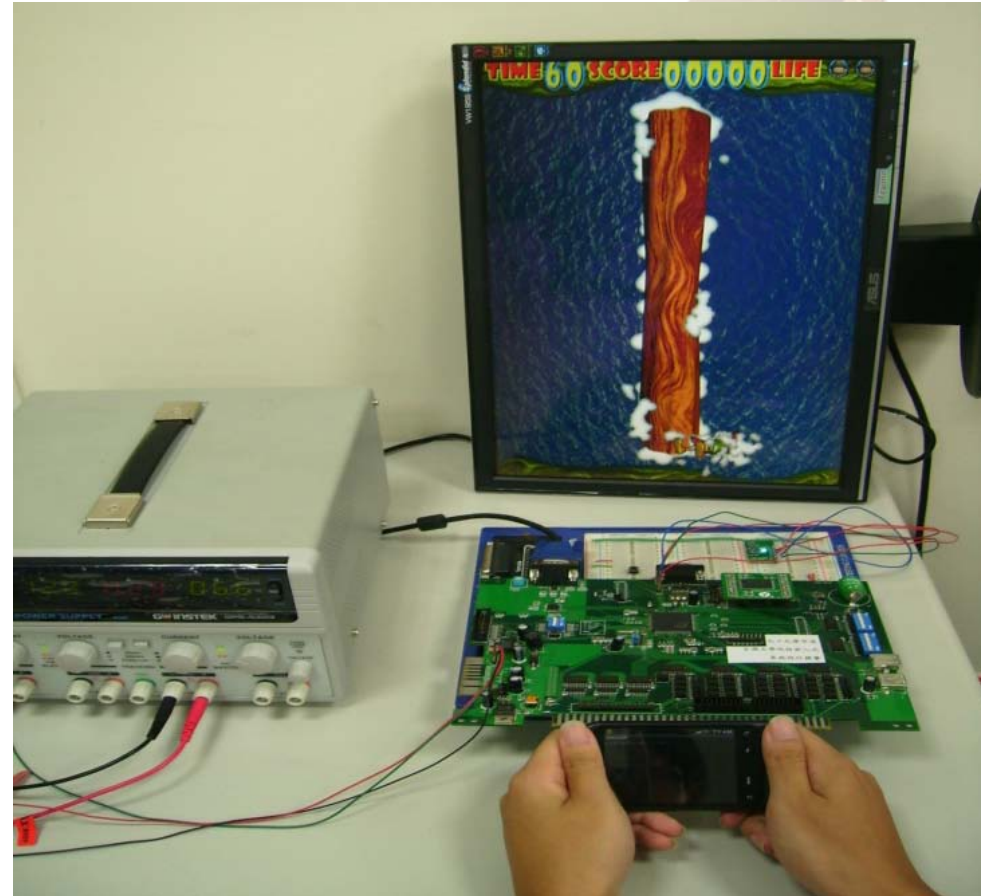
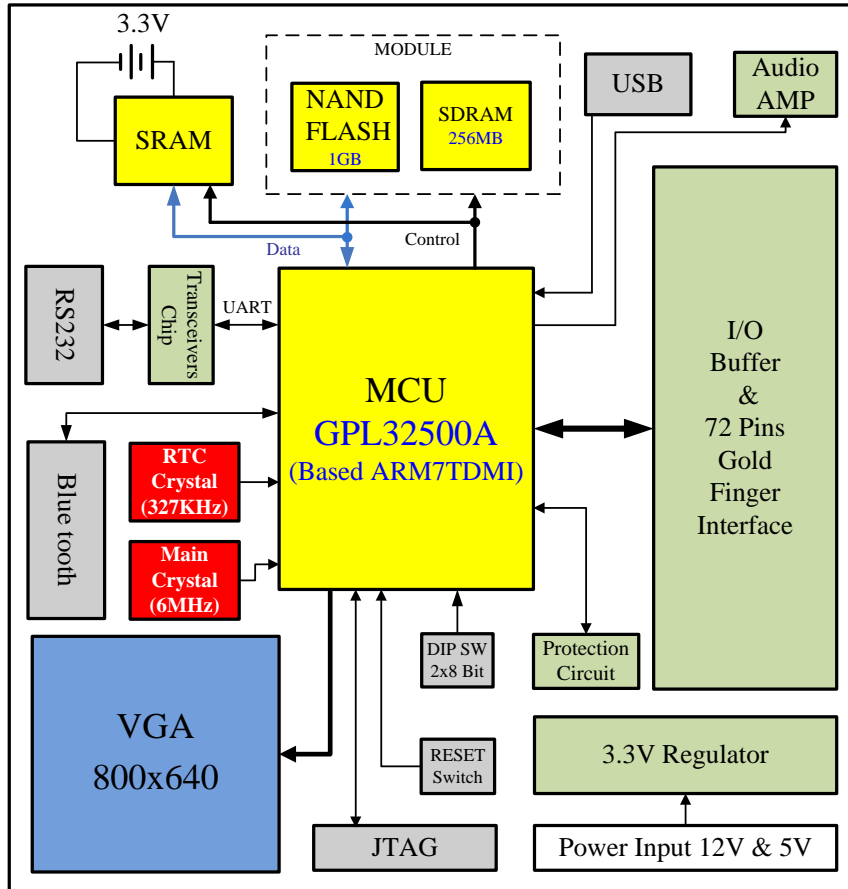


Video

經濟部標準檢驗局電磁相容(EMC)設計競賽



Embedded Development Platform

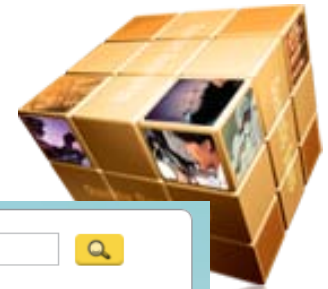


IC Samples



- ❖ Linear Technology: <http://www.linear.com/>
- ❖ Analog Device: <http://www.analog.com>
- ❖ T.I.: <http://www.ti.com>
- ❖ NXP: <http://www.classic.nxp.com>
- ❖ Maxim: <http://www.maxim-ic.com/>
- ❖ Free Scale: <http://www.freescale.com/>

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OVERVIEW

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LTC4261 - Negative Voltage Hot Swap Controllers with ADC and I2C Monitoring

LTC3455/LTC3455-1 - Dual DC/DC Converter with USB Power Manager and Li-Ion Battery Charger

Features

- Seamless Transition between Input Power Sources: Li-Ion Battery, USB, and 5V Wall Adapter
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- 4.1V Float Voltage (LTC3455-1) Improves Battery Life and High Temperature Safety Margin
- Hot Swap Output for SDIO and Memory Cards
- Pin-Selectable Burst Mode Operation
- Output Disconnect: All Outputs Discharged to Ground During Shutdown
- Available in a 4mm x 4mm x 0.75mm 24-Pin QFN Package

Typical Application

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DOCUMENTATION

Datasheet

- 1 LTC3455/LTC3455-1 - Dual DC/DC Converter with USB Power Manager and Li-Ion Battery Charger

Design Note

- 1 DN1008 - Simple, Efficient, All-in-One USB Power Management IC Solution

Reliability Data

- 1 R415 - Reliability Data

LT Journal

- 1 Feb 2004 Complete USB Power Manager, Li-Ion Charger and Two Buck Converters in a 4mm x 4mm QFN
- 1 September 2008 - New Family of Integrated Power Controllers Combine Fast Battery Charging, PowerPath Control and Efficient DC/DC

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Xilinx and Analog Devices Achieve JEDEC JESD204B Interoperability (24 Sep 13)

Analog Devices Achieves Major Milestone by Shipping 1 Billionth Channel of iCoupler Digital Isolation (19 Sep 13)

Analog Dialogue (Sept 2013) Features: Design and Debug a PLL, Multiplexed 3-Wire RTD Measurement, and Get Answers at EngineerZone (17 Sep 13)

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Webcast

Industrial Process Control: Communication Solutions

Webcast

Got my data over the isolation barrier! Now how do I get power to run it?

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| Min | 14.0 V | Max | 22.0 V |
| Vin | | Vout | 3.3 V |
| Output | | Iout | 2.0 A |
| Ambient Temp | | | 30 °C |
| Multiple Loads | | Single Output | |
| Power Architect | | Start Design | |

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BOURNS[®]

TCS 元件

SILICON LABS

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