系統晶片設計與應用

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Outline

1. Integrated Circuit
2. Chip Design
3. Application

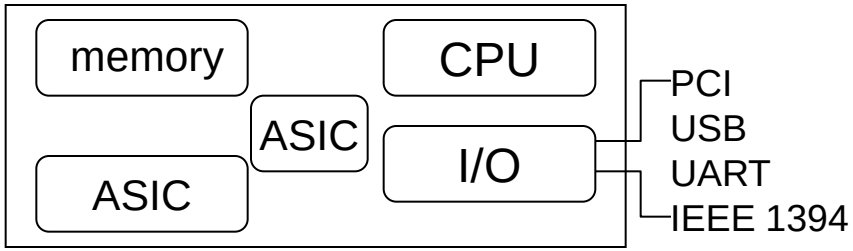
Hardware Implementation

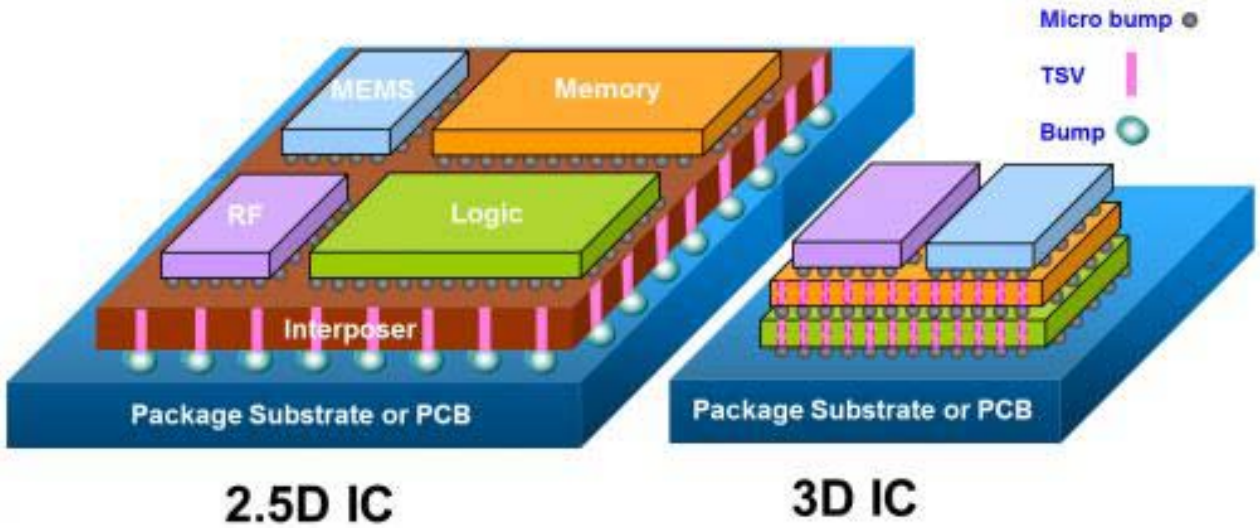
Methods or Algorithms can be implemented with

1. Hardware processor + suitable software programs (flexibility)
   a. Pentium IV + suitable software programs (high-level language)
   b. TI-DSP + suitable software programs
   c. MCU(8051) + suitable software programs (low-level language)
2. Dedicated hardware circuits (faster)
   a. old_PCBs (TTL SSI, MSI chips and wires)
   b. new_PCBs(some devices, application specific integrated circuit-ASIC, wires)

Hardware Implementation

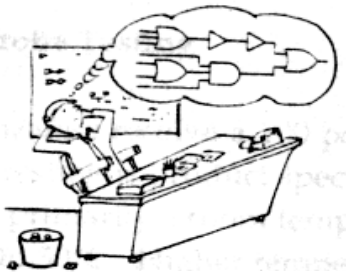
3. Some hardware circuits + software programs (to solve more complex problems)
   a. System on a board (memory, processor, ASIC, I/O, other devices)
   b. System on a chip (SoC)
   c. current and future work (3D IC)

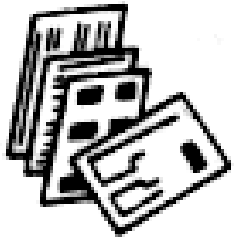


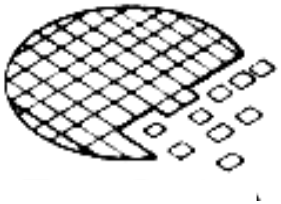


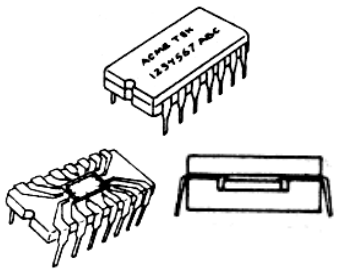
Ref：CTIMES/新聞/積極創新 台積電獲2013百大創新機構殊榮

IC Industry in Taiwan









邏輯設計　光罩設計　晶粒測試及切割　封　裝　成品測試

設計 → 光罩 → 製造 → 封裝 → 測試

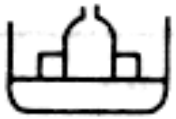
聯發科、晨星、聯詠、群聯、瑞昱、奇景 …

台灣光罩

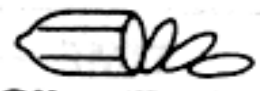
台積電、聯電

日月光、矽品

欣銓、京元電



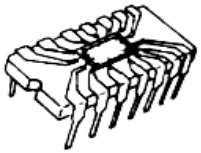
長晶



晶圓切割

中美晶、合晶、嘉晶

晶圓



QFP, TSOP, SOT, SOJ

導線架

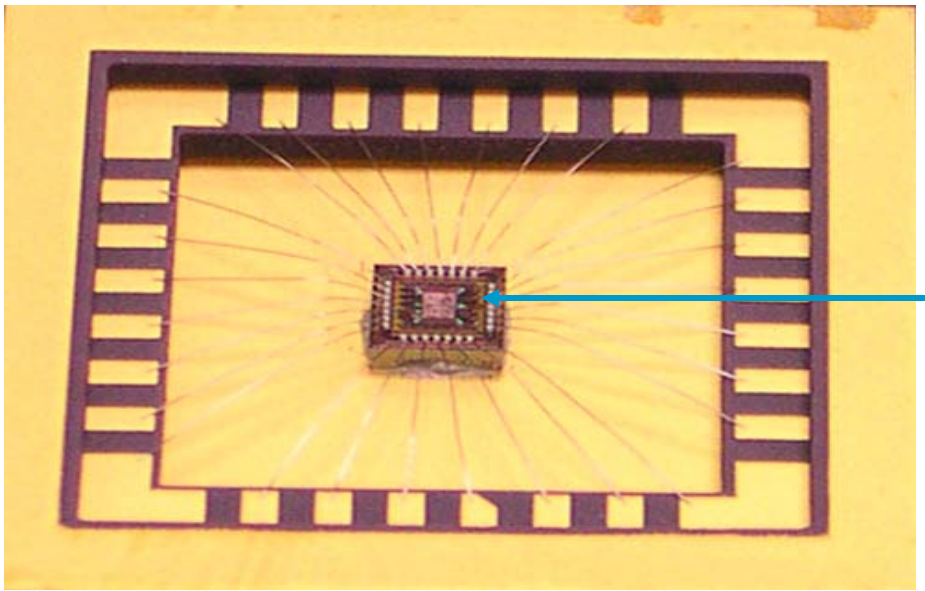
順德

化學品

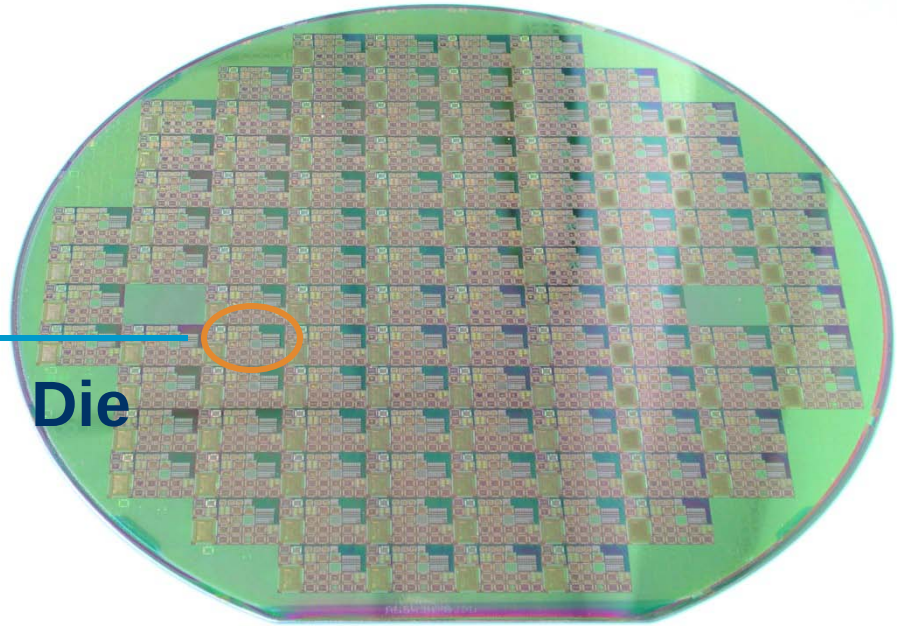
三福化工

Wafer & Die & Packaging

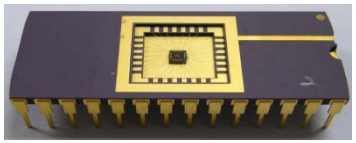
Packaging

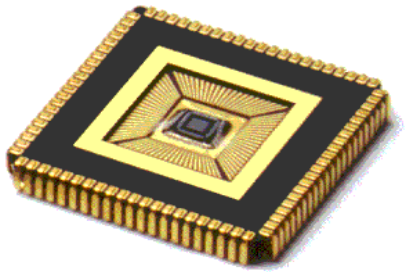


Wafer



Die



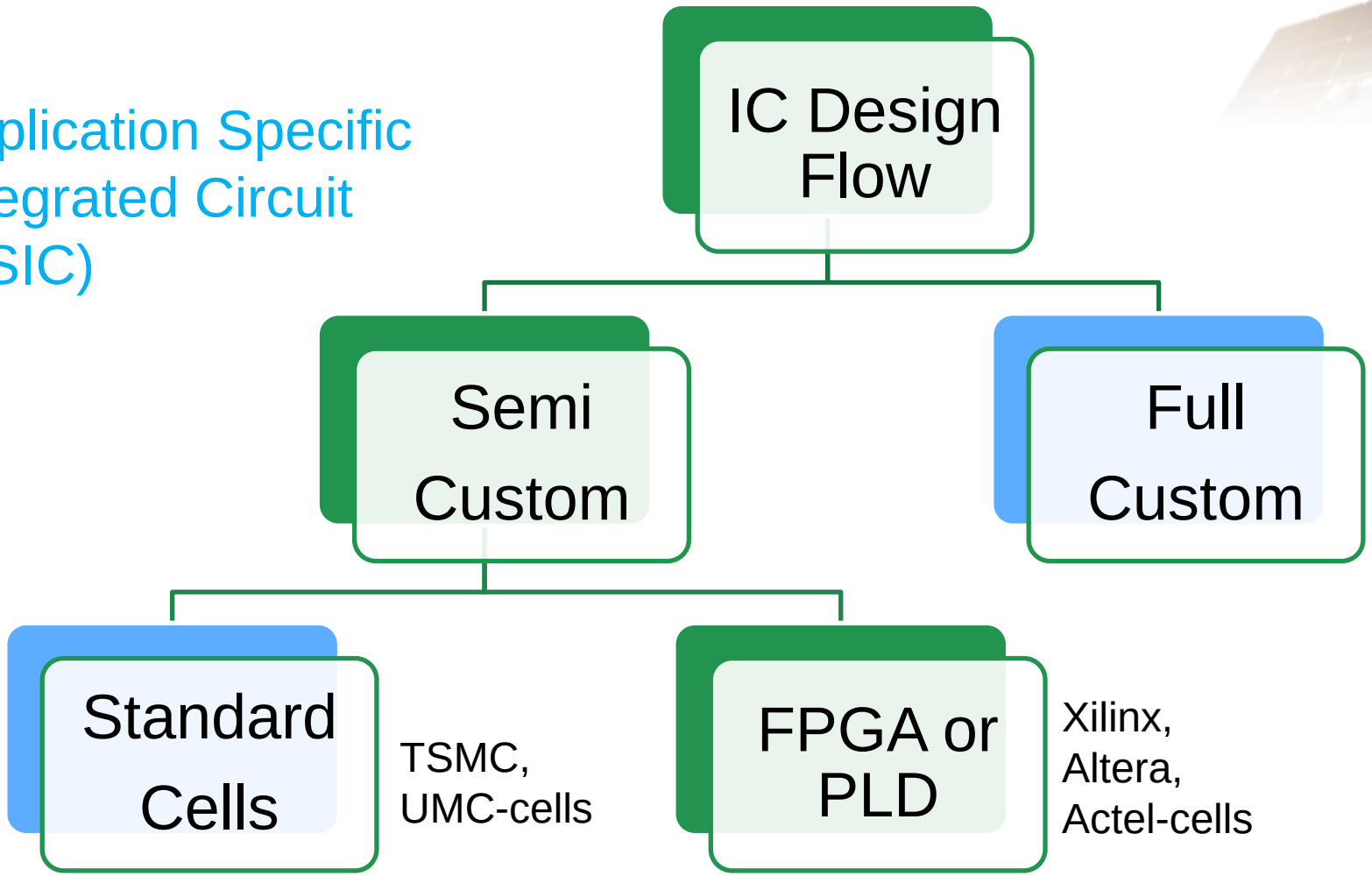


Outline

1. Integrated Circuit
2. Chip Design
3. Application

IC Design Flow

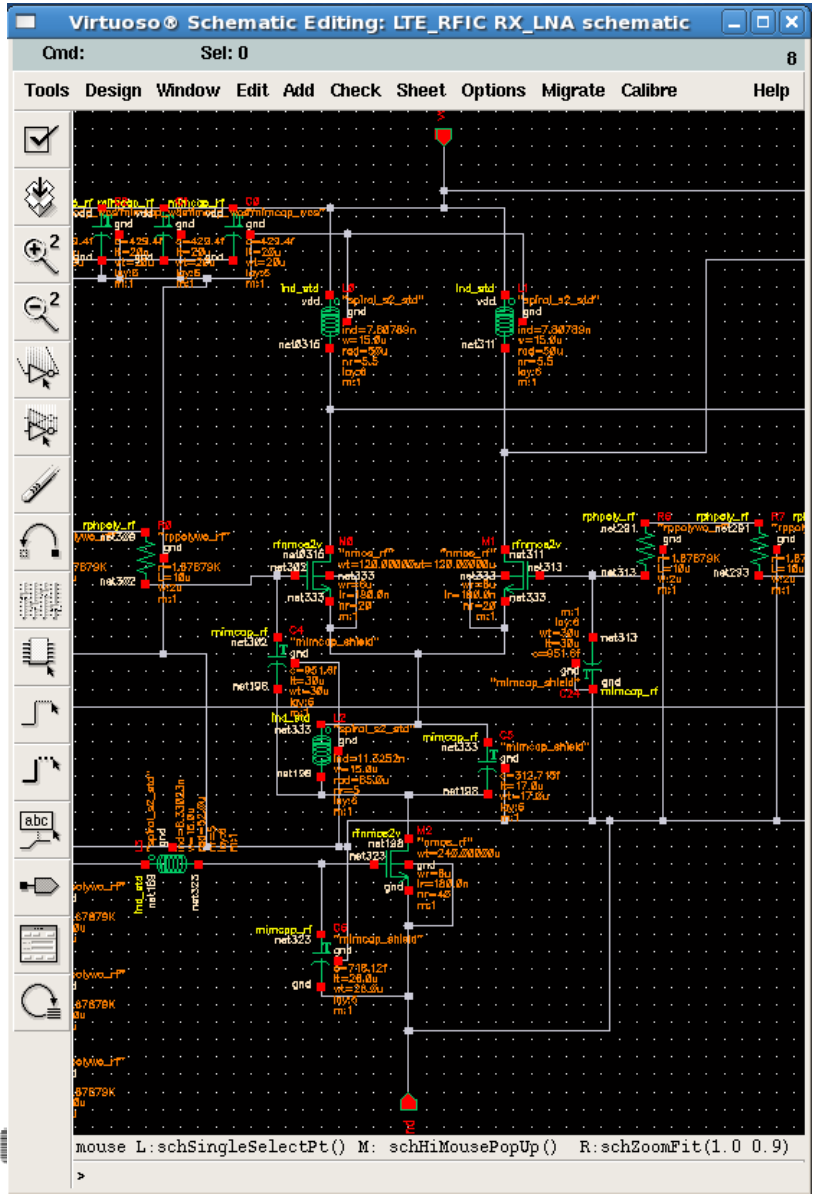
Application Specific Integrated Circuit (ASIC)

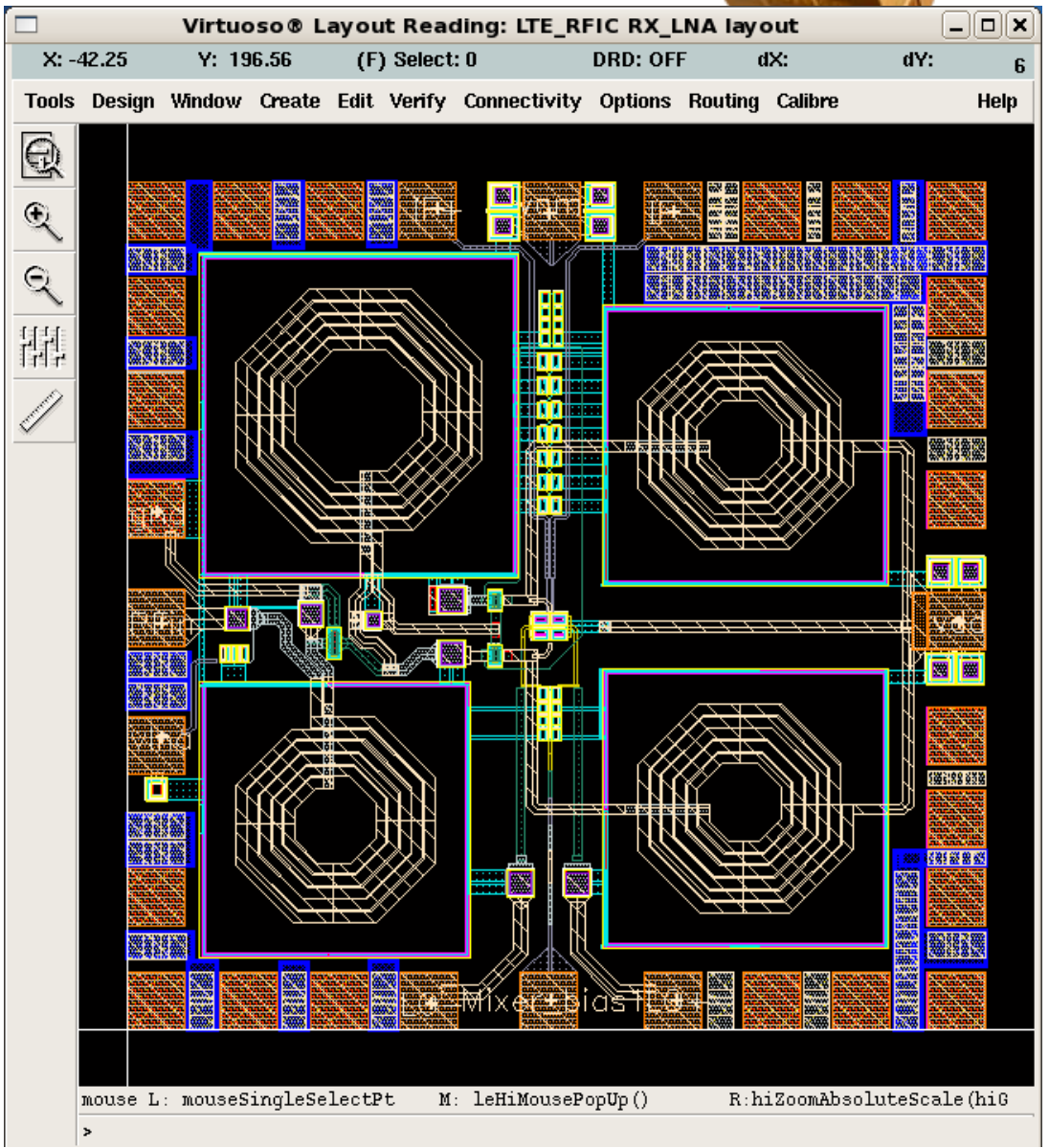


Full (Fully) Custom Design

- For analog circuits and digital circuits requiring custom optimization
- Gates, transistors and layout are designed and optimized by the engineer
- Full custom layout editor with Virtuoso

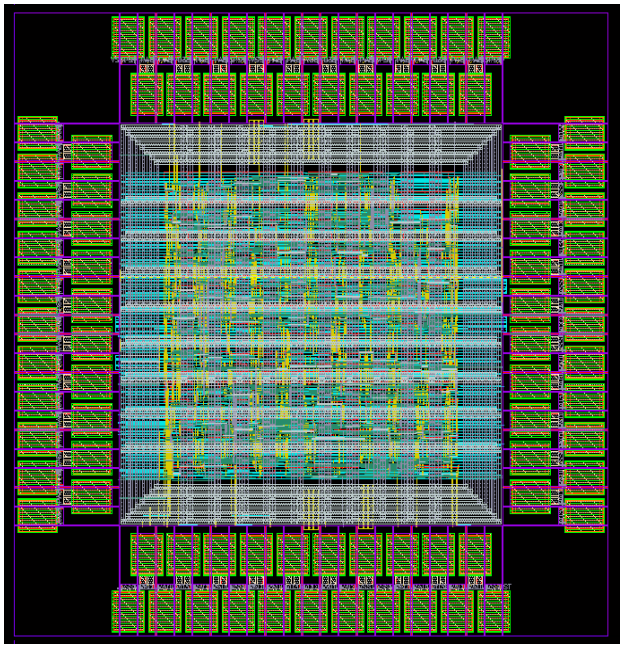
Full (Fully) Custom Design (Cont.)





Semi Custom Design

- For larger digital circuits
- Real gates, transistors and layout are synthesized and optimized by related software tools
- Realization with hardware description language (HDL) such as VHDL and Verilog



Semi Custom Design (Cont.)

a. Product specification
b. Modeling with HDL
c. Synthesis (by using suitable standard cell)
d. Simulation and verification
e. Physical placement and layout

-- implemented with suitable tools

f. Tape-out (real chip) -- implemented by suitable Fabrication companies
g. Testing -- implemented by suitable tools and mechanisms

more flexible, shorter design cycle, suitable for smaller production

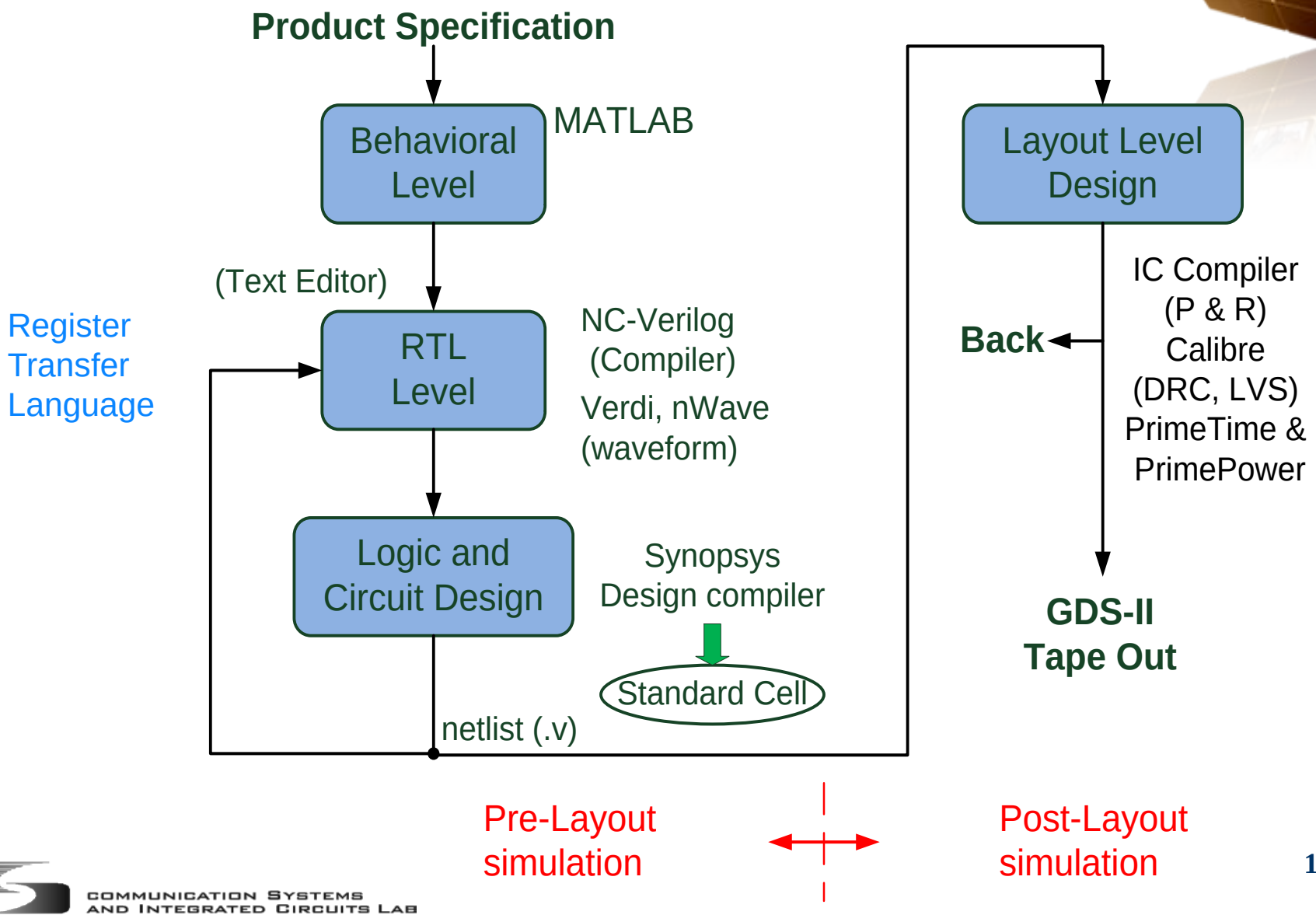
Two different solutions :

PLD → FPGA or CPLD — Xilinx, Altera

Standard cell → Real ASIC chip — Fab (TSMC, UMC, ..)

less flexible, long design cycle, larger-scale production to reduce price

Standard Cells



- Vendor Package

- - Cadence All
- - Mentor All
- - Synopsys All

AMS Verification

- Analog/Mixed Signal Design Flow
- Eldo
- HSPICE
- NanoSim
- SMASH
- Virtuoso Multi-Mode Simulation
- Virtuoso Spectre Circuit Simulator

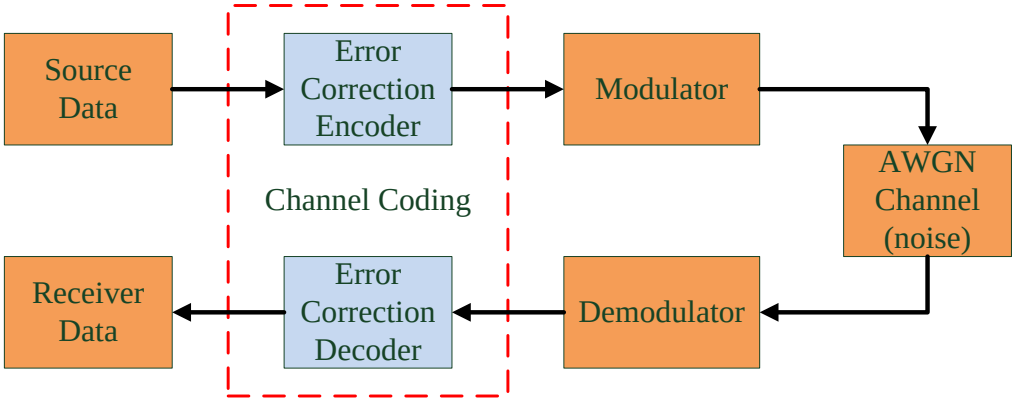
Cell Library

- Cell-Based Design Kit for IC Contest

Custom IC Design

- CosmosScope
- Custom Designer
- Laker Advanced Design Platform
- Laker Custom Layout Automation System
- SpiceExplorer
- Virtuoso AMS Designer
- Virtuoso Analog Design Environment
- Virtuoso NeoCircuit
- Virtuoso Schematic Editor

System Simulation

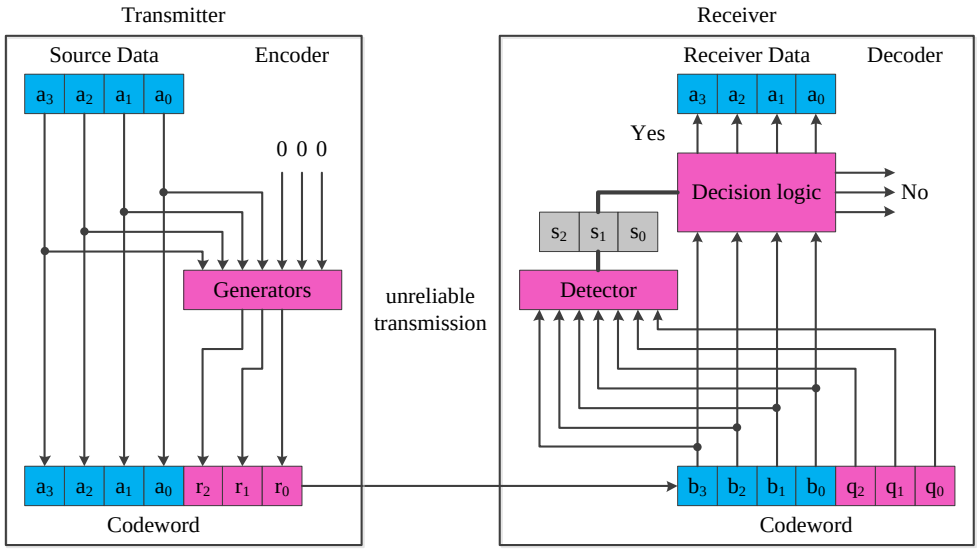


System Block Diagram

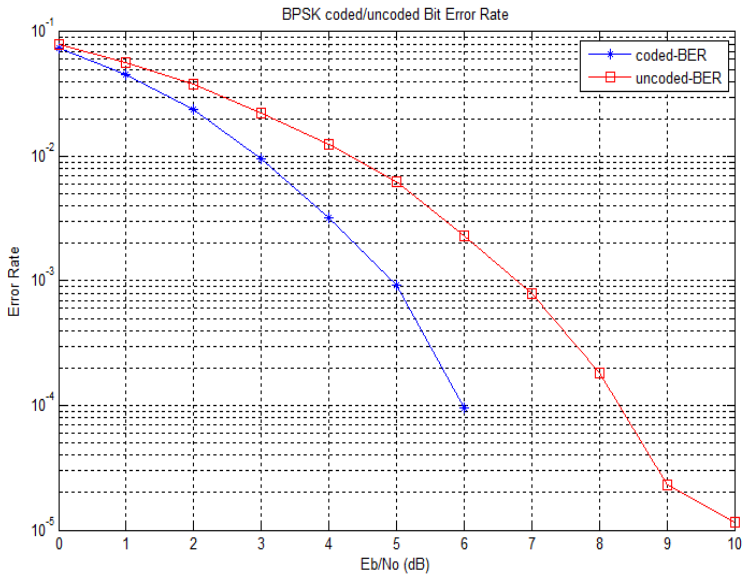
$$c(X) = c_0 + c_1 X + c_2 X^2 + \cdots + c_{n-1} X^{n-1}$$

$$X^i c(X) = X^i (c_0 + c_i X + \ldots\ldots + c_{n-i-1} X^{n-i-1} + c_{n-i} X^{n-i} + \ldots + c_{n-1} X^{n-1})$$
$$= c_0 X^i + c_i X^{i+1} + \ldots + c_{n-i-1} X^{n-1} + c_{n-i} X^n + \ldots\ldots + c_{n-1} X^{n+i-1}$$
$$= c_{n-i} X^n + \ldots + c_{n-1} X^{n+i-1} + c_0 X^i + c_1 X^{i+1} + \ldots + c_{n-i-1} X^{n-1}$$

Algorithms



Circuit Architecture



Simulation Result

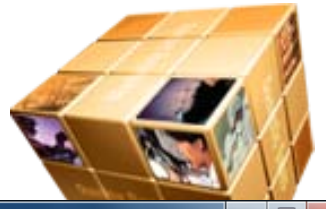
RTL Simulation

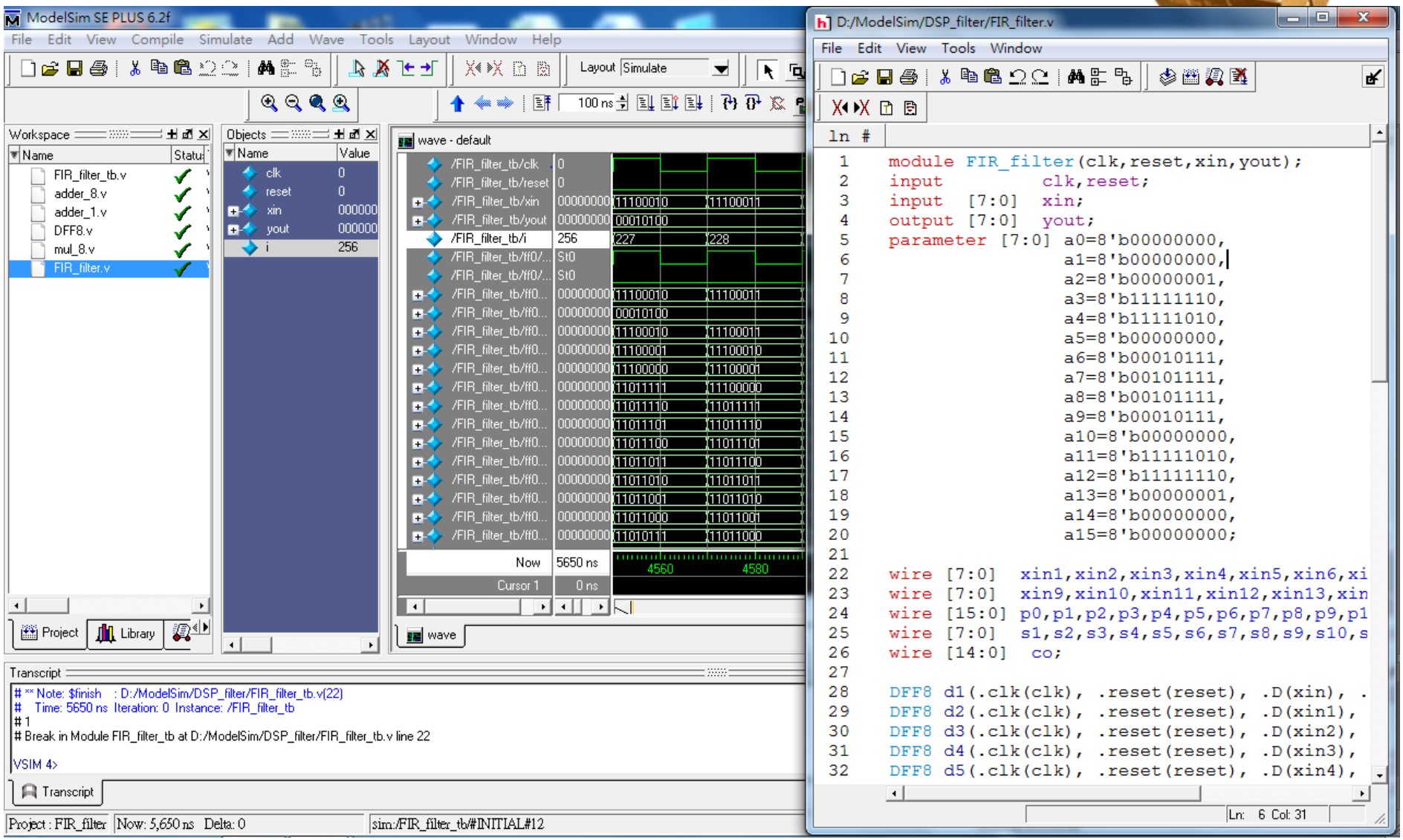
- Describe the circuits with Hardware Description Language (HDL) – Verilog-HDL, VHDL
- Verification and Analysis
  - Behavioral Simulation
  - Logic Simulation
  - Circuit Simulation
- ModelSim – Supported on Windows and Linux operating systems
- Verdi – Supported on Linux operating system

ModelSim®

SYNOPSYS®
Accelerating Innovation

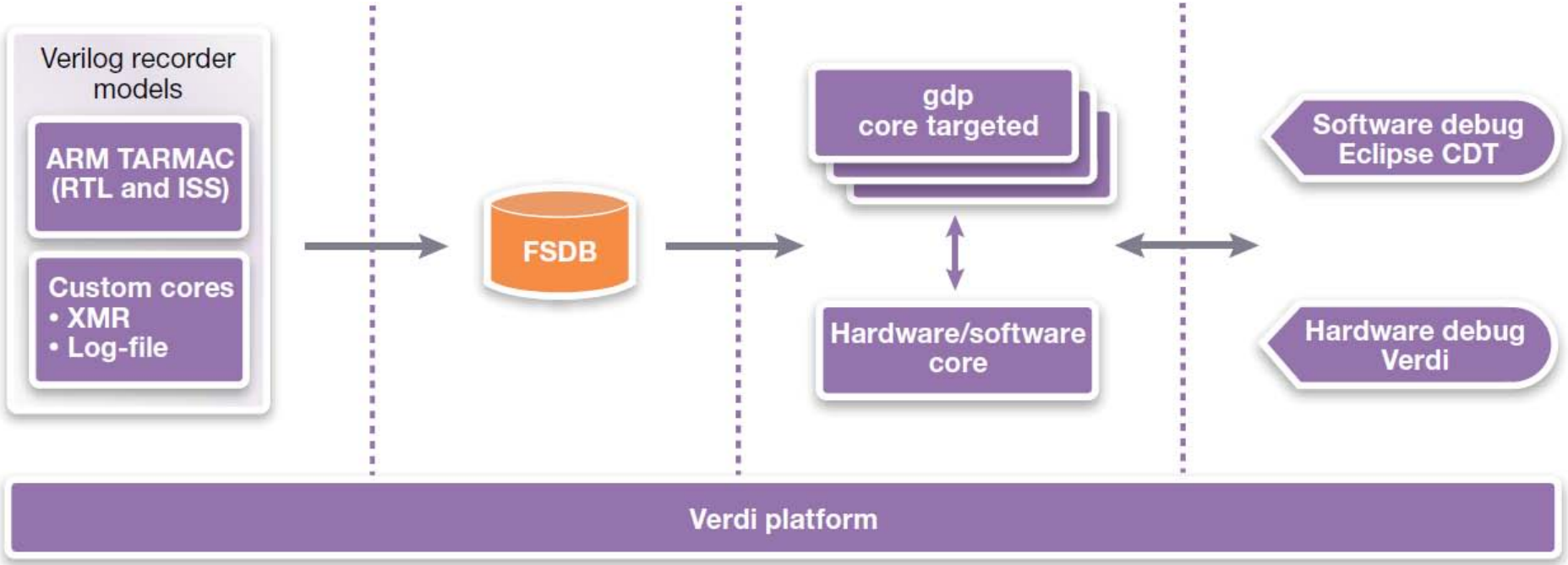
ModelSim



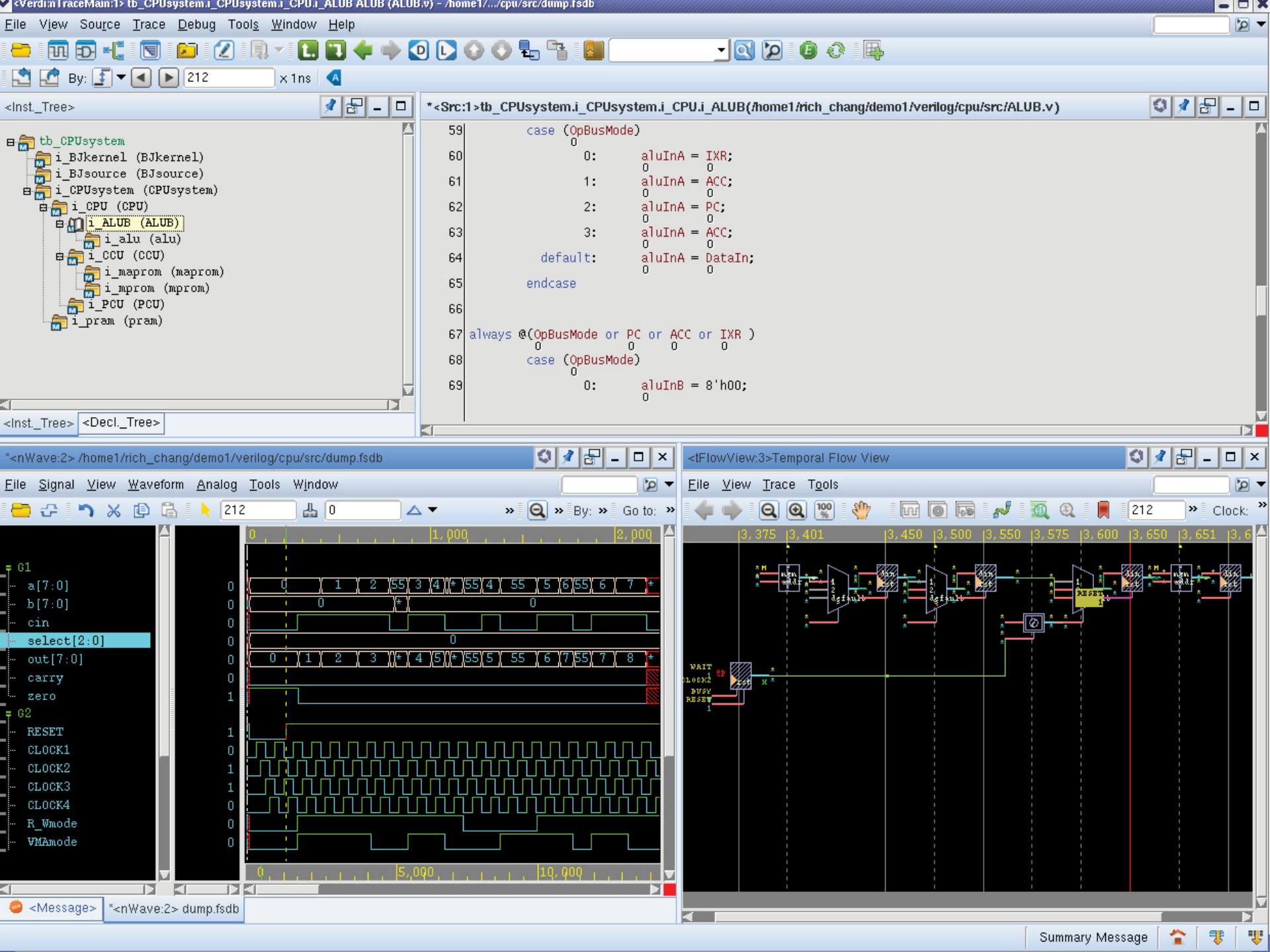

ModelSim SE PLUS 6.2f
File Edit View Compile Simulate Add Wave Tools Layout Window Help
Workspace
Name
FIR_filter_tb.v
adder_8.v
adder_1.v
DFF8.v
mul_8.v
FIR_filter.v
Project
Library
Objects
Name
Value
clk
reset
xin
yout
i
wave - default
/FIR_filter_tb/clk
/FIR_filter_tb/reset
/FIR_filter_tb/xin
/FIR_filter_tb/yout
/FIR_filter_tb/i
Now
5650 ns
Cursor 1
0 ns
wave
Transcript
** Note: $finish : D:/ModelSim/DSP_filter/FIR_filter_tb.v(22)
Time: 5650 ns Iteration: 0 Instance: /FIR_filter_tb
1
Break in Module FIR_filter_tb at D:/ModelSim/DSP_filter/FIR_filter_tb.v line 22
VSIM 4>
Transcript
Project : FIR_filter
Now: 5,650 ns Delta: 0
sim:/FIR_filter_tb/#INITIAL#12
D:/ModelSim/DSP_filter/FIR_filter.v
File Edit View Tools Window
ln #
1 module FIR_filter(clk,reset,xin,yout);
2 input clk,reset;
3 input [7:0] xin;
4 output [7:0] yout;
5 parameter [7:0] a0=8'b00000000,
6 a1=8'b00000000,
7 a2=8'b00000001,
8 a3=8'b11111110,
9 a4=8'b11111010,
10 a5=8'b00000000,
11 a6=8'b00010111,
12 a7=8'b00101111,
13 a8=8'b00101111,
14 a9=8'b00010111,
15 a10=8'b00000000,
16 a11=8'b11111010,
17 a12=8'b11111110,
18 a13=8'b00000001,
19 a14=8'b00000000,
20 a15=8'b00000000;
21
22 wire [7:0] xin1,xin2,xin3,xin4,xin5,xin6,xi
23 wire [7:0] xin9,xin10,xin11,xin12,xin13,xin
24 wire [15:0] p0,p1,p2,p3,p4,p5,p6,p7,p8,p9,p1
25 wire [7:0] s1,s2,s3,s4,s5,s6,s7,s8,s9,s10,s
26 wire [14:0] co;
27
28 DFF8 d1(.clk(clk), .reset(reset), .D(xin), .
29 DFF8 d2(.clk(clk), .reset(reset), .D(xin1),
30 DFF8 d3(.clk(clk), .reset(reset), .D(xin2),
31 DFF8 d4(.clk(clk), .reset(reset), .D(xin3),
32 DFF8 d5(.clk(clk), .reset(reset), .D(xin4),
Ln: 6 Col: 31

HDL Debugging with Verdi

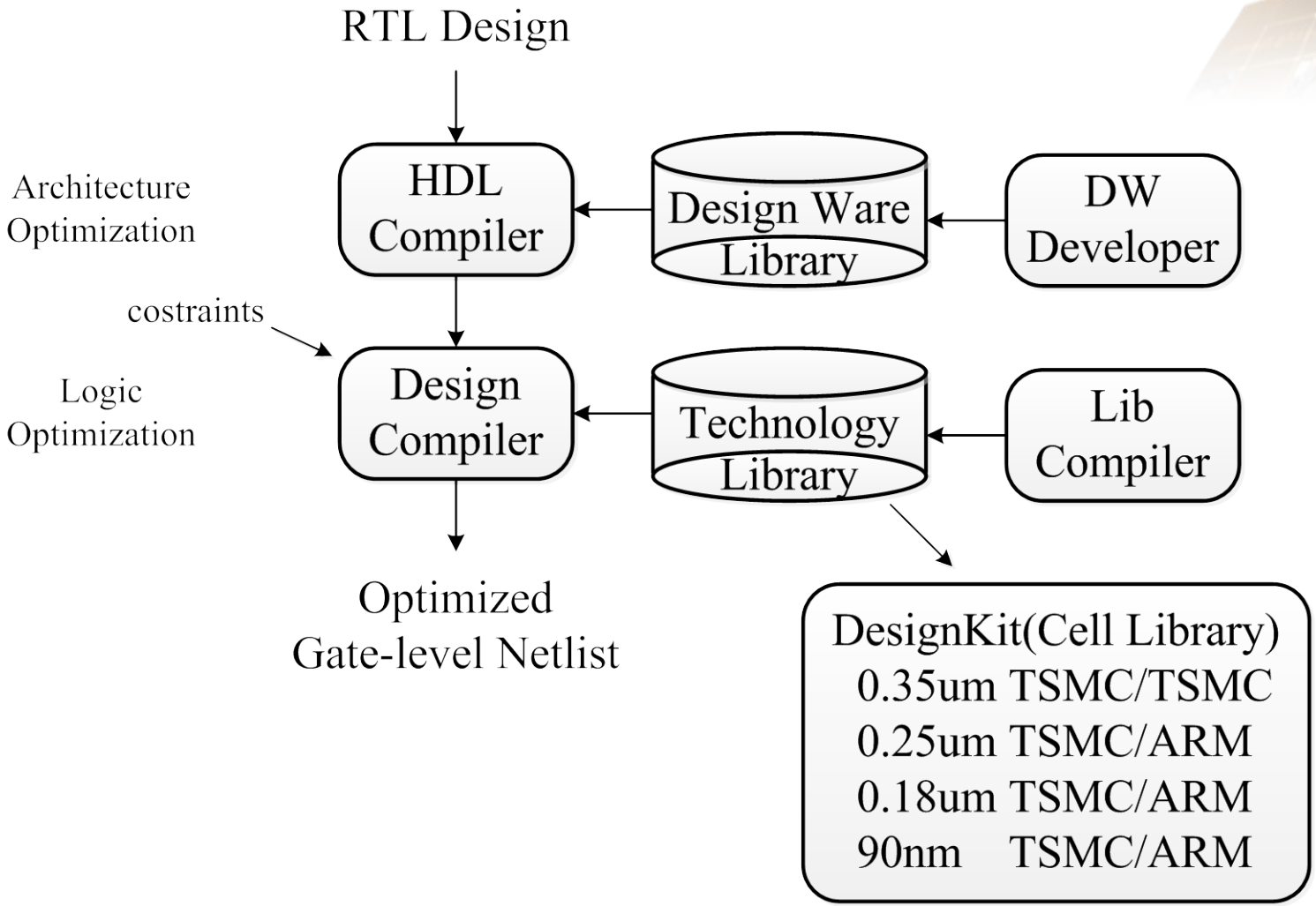
- The Verdi system lets you focus on tasks that add more value to your designs by cutting your debug time, typically by over 50%



Ref：Synopsys Debug
https://www.synopsys.com/Tools/Verification/debug/Pages/default.aspx


<Verdi:nTraceMain:1> tb_CPUsystem.i_CPUsystem.i_CPU.i_ALUB ALUB (ALUB.v) - /home1/.../cpu/src/dump.fsdb
File View Source Trace Debug Tools Window Help
By: 212 x 1ns
<Inst._Tree>
tb_CPUsystem
i_BJkernel (BJkernel)
i_BJsource (BJsource)
i_CPUsystem (CPUsystem)
i_CPU (CPU)
i_ALUB (ALUB)
i_alu (alu)
i_CCU (CCU)
i_maprom (maprom)
i_mprom (mprom)
i_PCU (PCU)
i_pram (pram)
<Inst._Tree> <Decl._Tree>
*<Src:1>tb_CPUsystem.i_CPUsystem.i_CPU.i_ALUB(/home1/rich_chang/demo1/verilog/cpu/src/ALUB.v)
59 case (OpBusMode)
60 0: aluInA = IXR;
61 1: aluInA = ACC;
62 2: aluInA = PC;
63 3: aluInA = ACC;
64 default: aluInA = DataIn;
65 endcase
66
67 always @(OpBusMode or PC or ACC or IXR)
68 case (OpBusMode)
69 0: aluInB = 8'h00;
*<nWave:2> /home1/rich_chang/demo1/verilog/cpu/src/dump.fsdb
File Signal View Waveform Analog Tools Window
212 0 By: Go to:
G1
a[7:0]
b[7:0]
cin
select[2:0]
out[7:0]
carry
zero
G2
RESET
CLOCK1
CLOCK2
CLOCK3
CLOCK4
R_Wmode
VMAmode
1,000
2,000
5,000
10,000
<Message> *<nWave:2> dump.fsdb
<tFlowView:3>Temporal Flow View
File View Trace Tools
212 Clock:
3,375 3,401 3,450 3,500 3,550 3,575 3,600 3,650 3,651
WAIT
CLOCK2
BUSY
RESET
Summary Message

Logic Synthesis with Design Compiler



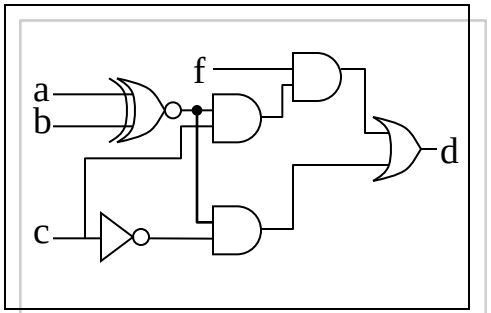
Synthesis

- *Synthesis = Translation+Optimization+Mapping*

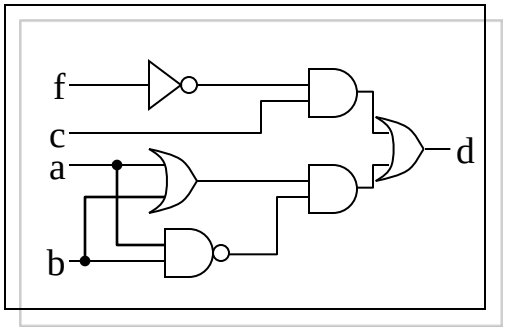
```
always @(…)
   if (a==b)
      if (c==1)
         d=f;
      else
         d=1;
   else
      d=0;
```

HDL Source

Translate into Boolean Representation



Optimize + Map

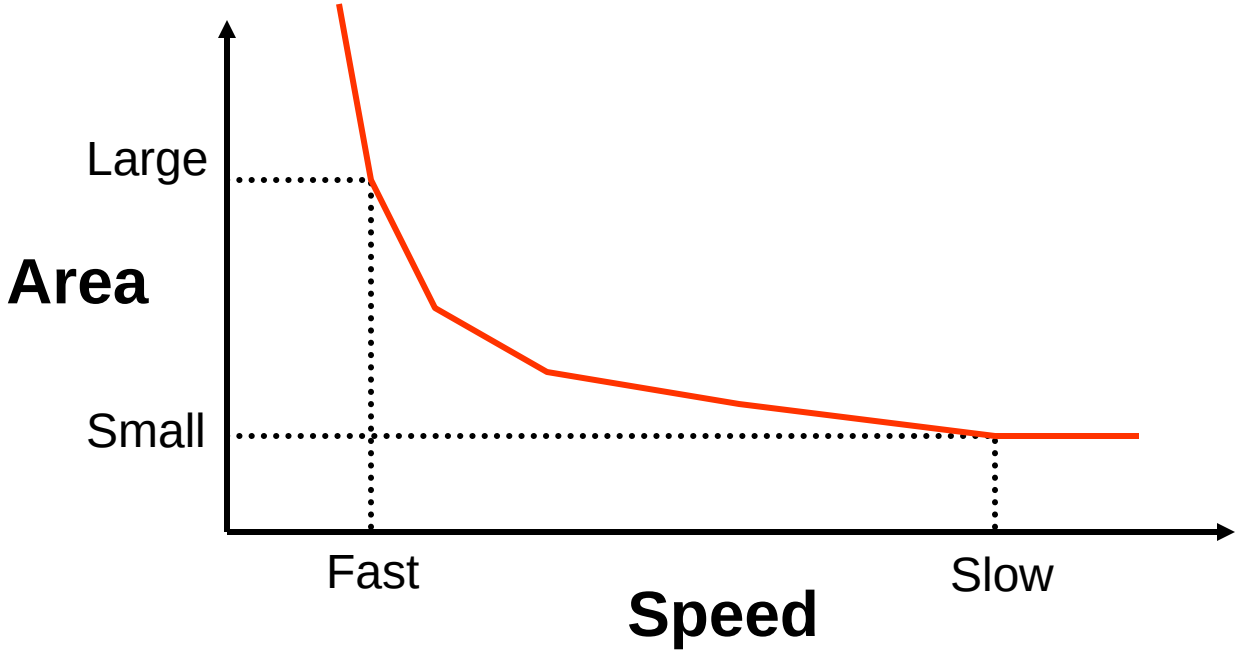


Target Technology

Process of logic synthesis

Synthesis (Cont.)

- Synthesis is **constraint-driven**
  - You set the goals. Design Compiler optimizes design toward goals.



Synthesis (Cont.)

Design Vision - TopLevel.1 (CHIP)

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help

CHIP

Hier.1

Logical Hier

Cells (Hierarchical)

Cell Name	Ref Name	Cell Path	D
c1	ECC_v4	c1	u..

Report.1 - Timing

```
  data required time                                    9.00
  ----------------------------------------------------------
  data required time                                    9.00
  data arrival time                                    -8.97
  ----------------------------------------------------------
  slack (MET)                                           0.03


***** End Of Report *****
```

Hier.1 Report.1

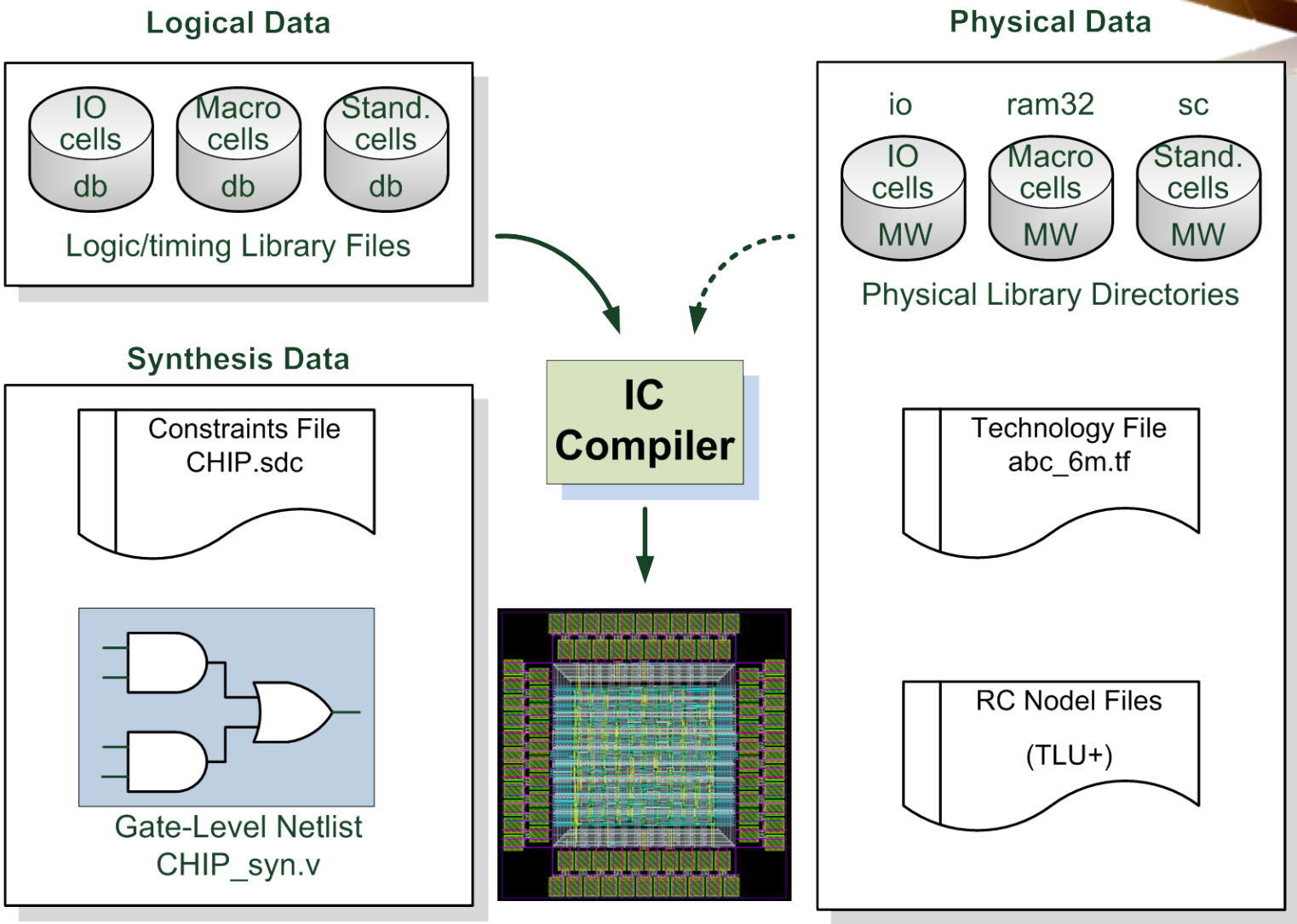
```
1
Current design is 'CHIP'.
design_vision> uplevel #0 { report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -
Information: Updating graph... (UID-83)
Information: Updating design information... (UID-85)
```

Log History Options:

design_vision>

Ready

Cell-Based IC Physical Design and Verification with IC Compiler

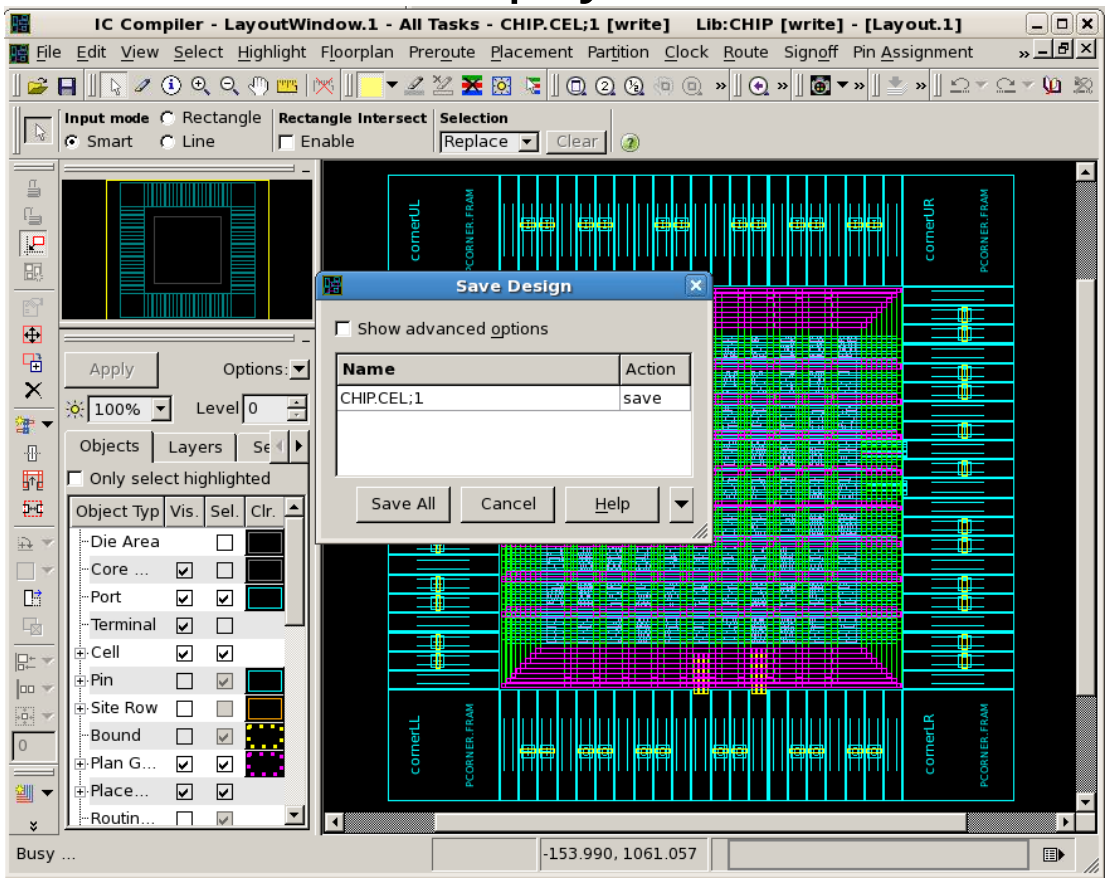


Placed, Routed & Optimized Design with Clock Trees

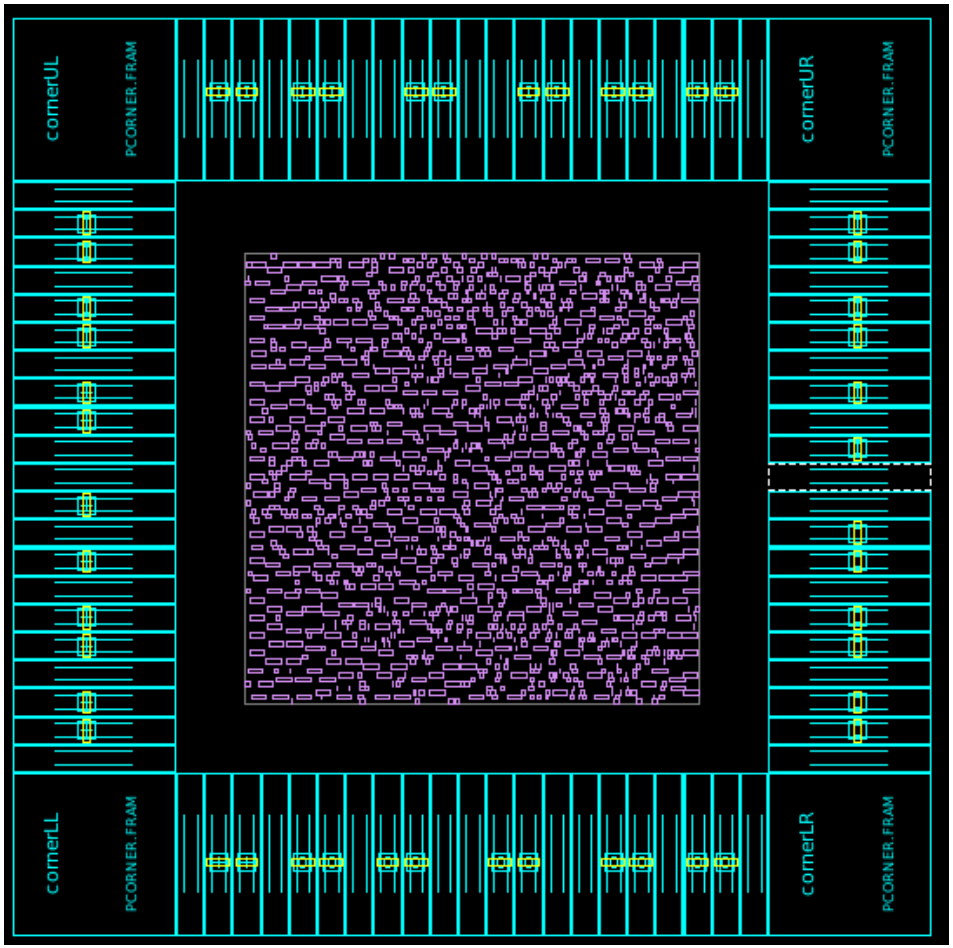
IC Compiler Flow

- Synthesis
- Design Setup
- Design Planning
- Placement
- CTS
- Routing
- CHIP Finishing

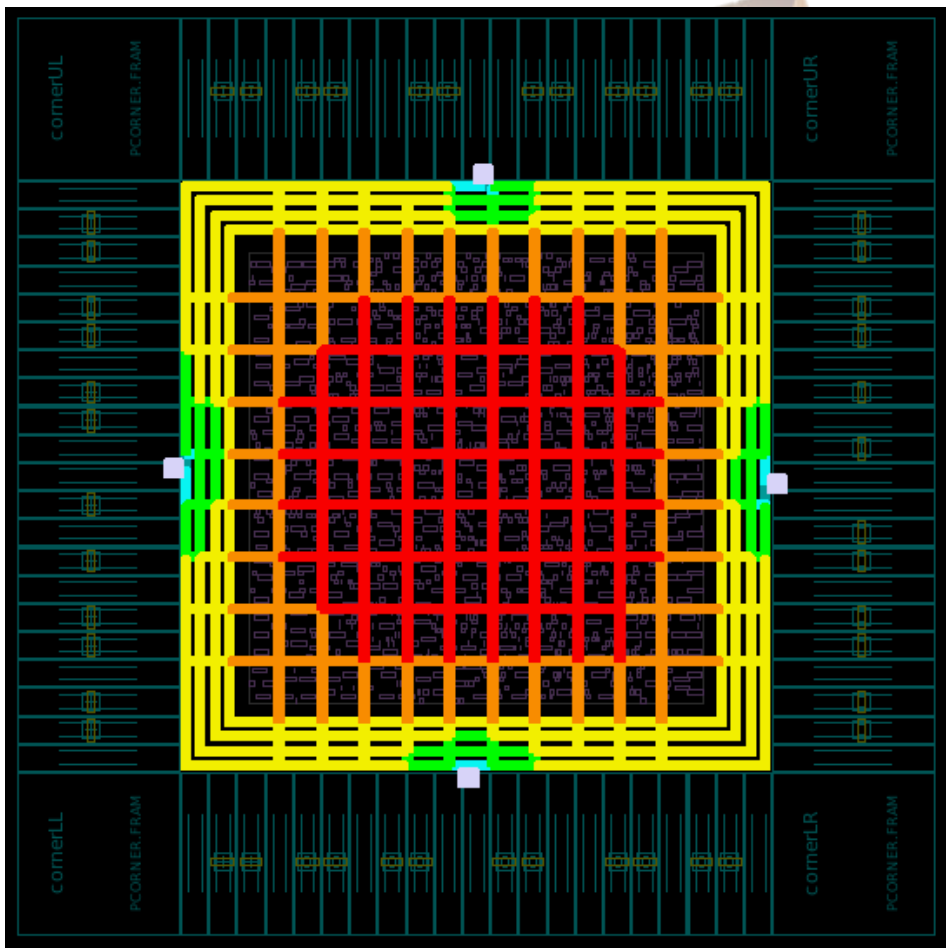
- Tcl or GUI-based user interface
- All Design Compiler reports enhanced with physical information



Placement

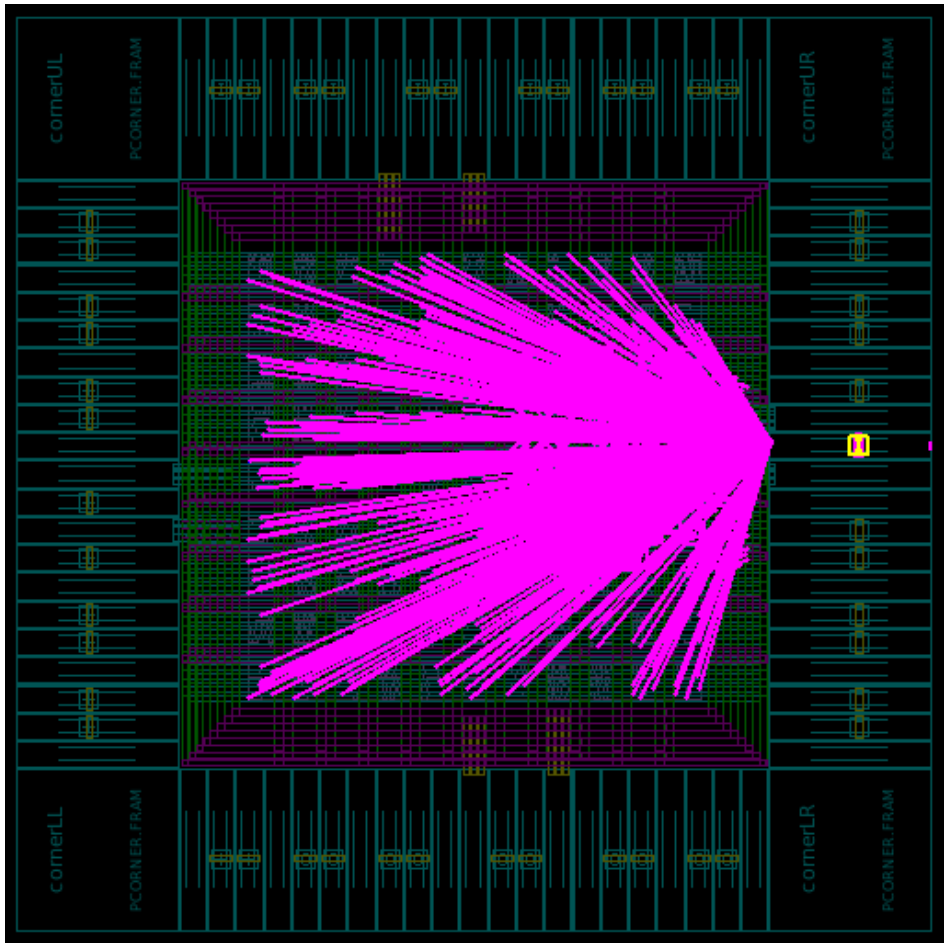


Floor plan

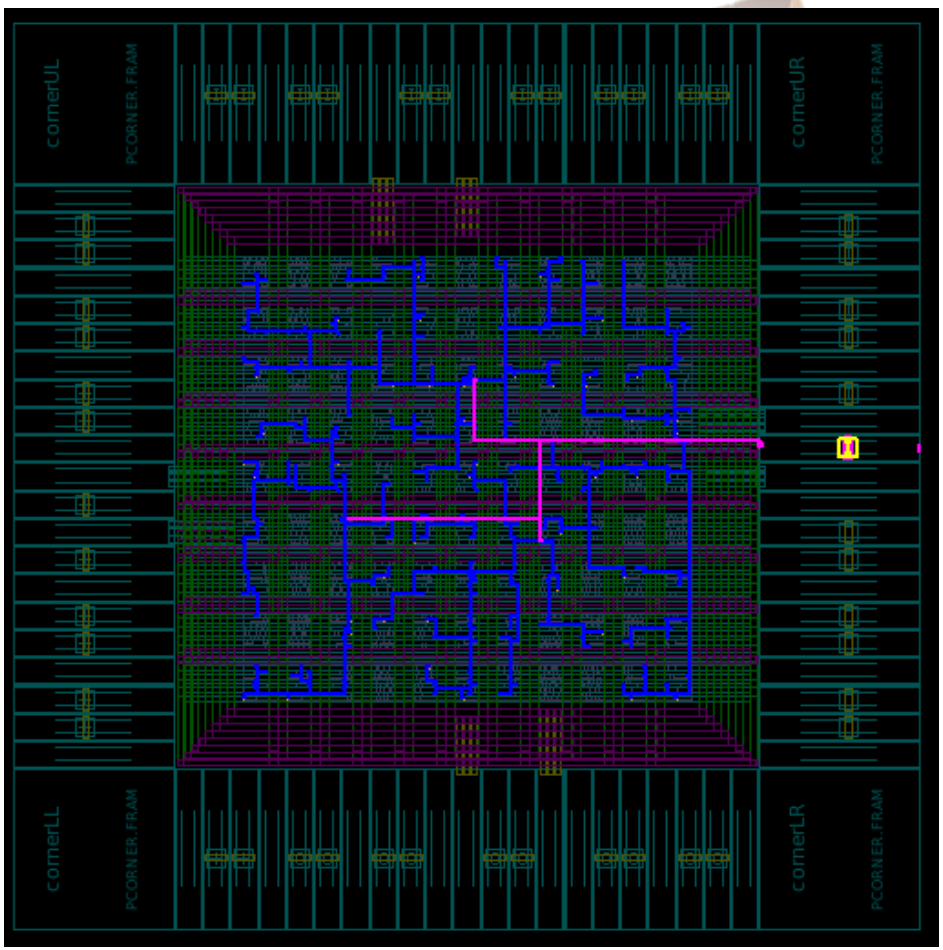


Power plan

Clock Tree Synthesis

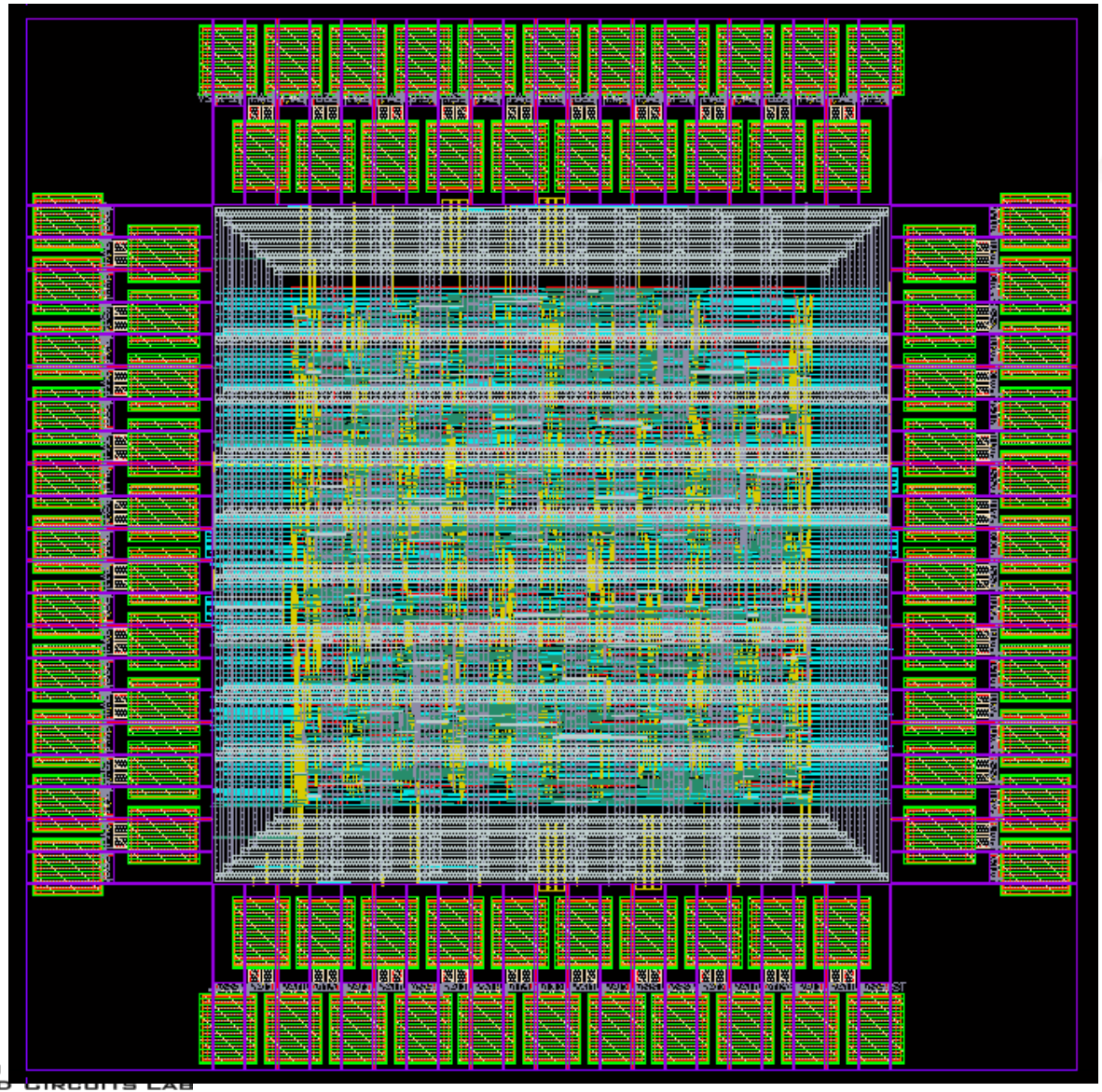


Before CTS



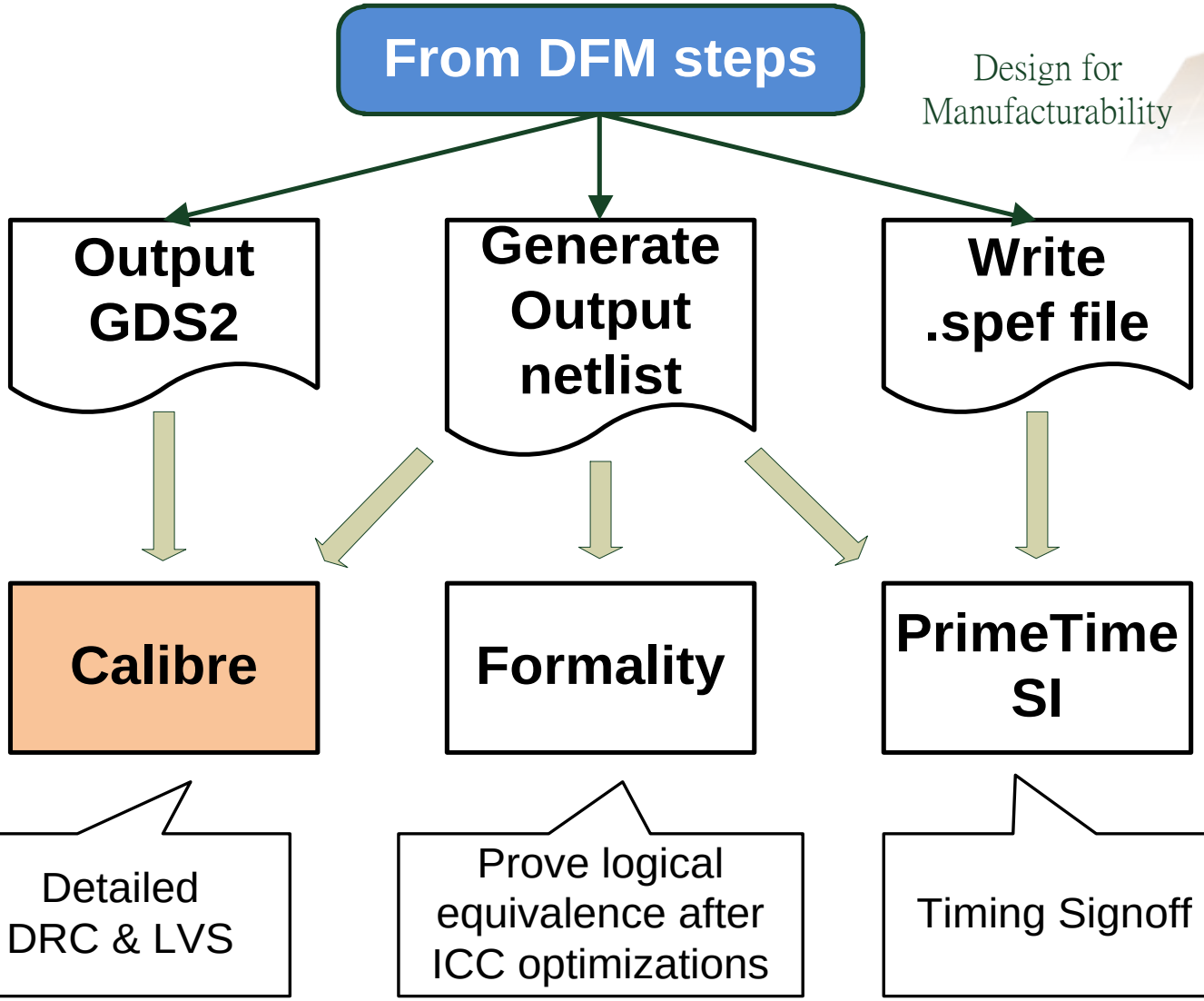
After CTS

Routing



Final Validation

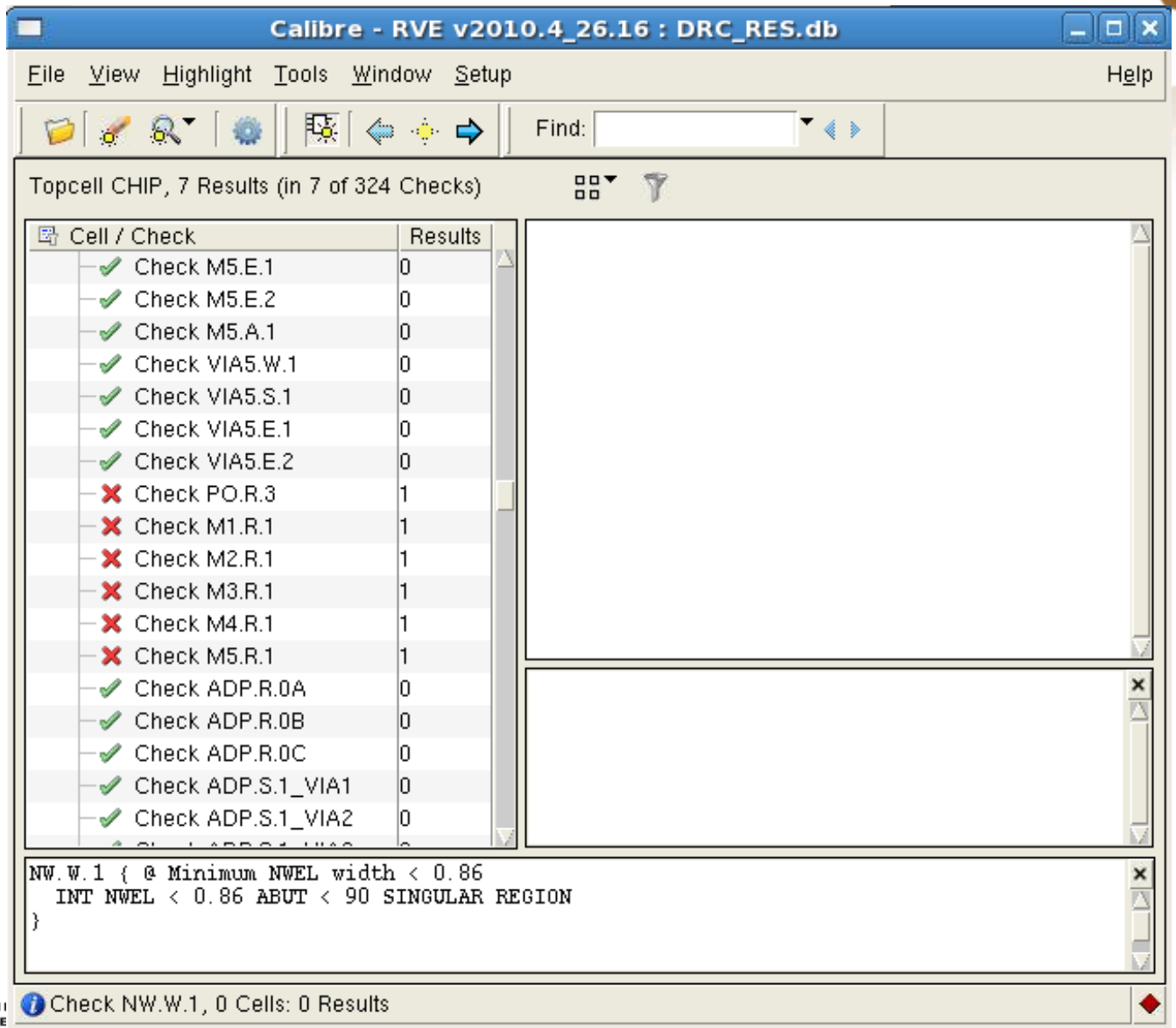
Design for Manufacturability



Calibre

- **Push button access to Calibre**
  - DRC, LVS, xRC
- **Shorter iteration time**
  - Direct invocation from design environment
  - Rapid verification & parasitic extraction
  - Easy location of results in design environment
  - Faster repair of errors & discrepancies
  - Parasitic visualization
- **Shorter time to tape-out**

Design Rule Check



Layout Versus Schematic

lvs.rep (~/IC/ICC/verifty/lvs) - gedit

檔案(F) 編輯(E) 顯示(V) 搜尋(S) 工具(T) 文件(D) 求助(H)

新增 開啓 儲存 列印... 復原 取消復原 剪下 複製 貼上 尋找 取代

CHIP_route.v × lvs.rep ×

```
                    CELL COMPARISON RESULTS ( TOP LEVEL )


                         #       ####################          _   _
                       #         #                  #         *   *
                     #   #       #     CORRECT      #           |
                      # #        #                  #         \___/
                       #         ####################                |


  Warning:  Ambiguity points were found and resolved arbitrarily.
  Warning:  LVS property resolution maximum exceeded.

LAYOUT CELL NAME:          CHIP
SOURCE CELL NAME:          CHIP
```

正在儲存檔案 '/home/ms/csictest/IC/ICC/verifty/lvs/lvs.rep' ... 第 360 行第 68 字 插入

Queue Server

❖ Online DRC

CIC 工作站使用申請表(EPIC)

姓名:
學校:國立勤益科技大學
系所:電子所
指導教授:林光浩
電話:
傳真:
E-Mail:

新增 Queue 帳號
製程名稱:
設計名稱:
連接到 Queue 的遠端主機:
連接到 Queue 的遠端帳號:

延長 Queue 帳號使用時間
Queue 伺服器帳號:
申請延長使用時間原因:

增加 Queue 帳號 Quota 大小
Queue 伺服器帳號:
增加 Quota 大小:
增加 Quota 原因:

送出申請表 重填

終端機

檔案(F) 編輯(E) 顯示(V) 終端機(T) 分頁(B) 求助(H)

```
################################################################################
#                                                                              #
#      主旨:因應 Queue server系統微調作業，暫停服務公告                       #
#                                                                              #
#      因應Queue server設備系統微調作業，預計時間為101/4/24(星期二)           #
#                                                                              #
#      ~ 101/5/1(星期二)，屆時Queue Server對外服務將暫停。                    #
#                                                                              #
#      造成不便，敬請見諒!若有重要行程執行請避開上述停機時間!!!               #
#                                                                              #
#                                                                              #
#      系統管理員 101.4.24                                                     #
#                                                                              #
################################################################################
queue.cic.org.tw ~> ls
2.01_CHIP_ECC.gds                          result_12-2-21_cicq78f_DRC_queue_9349
result_12-2-18_cicq78f_DRC_queue_2615      result_12-2-21_cicq78f_LPE_queue_9390
result_12-2-18_cicq78f_LPE_queue_2548      result_12-3-6_cicq78f_DRC_queue_4120
result_12-2-18_cicq78f_LPE_queue_2828
queue.cic.org.tw ~> Qentry -M DRC -tech TSMC18 -f 2.01_CHIP_ECC.gds -T CHIP -c T
SMC18 -i TSMC18 -addTagCell -addDummyCell
```

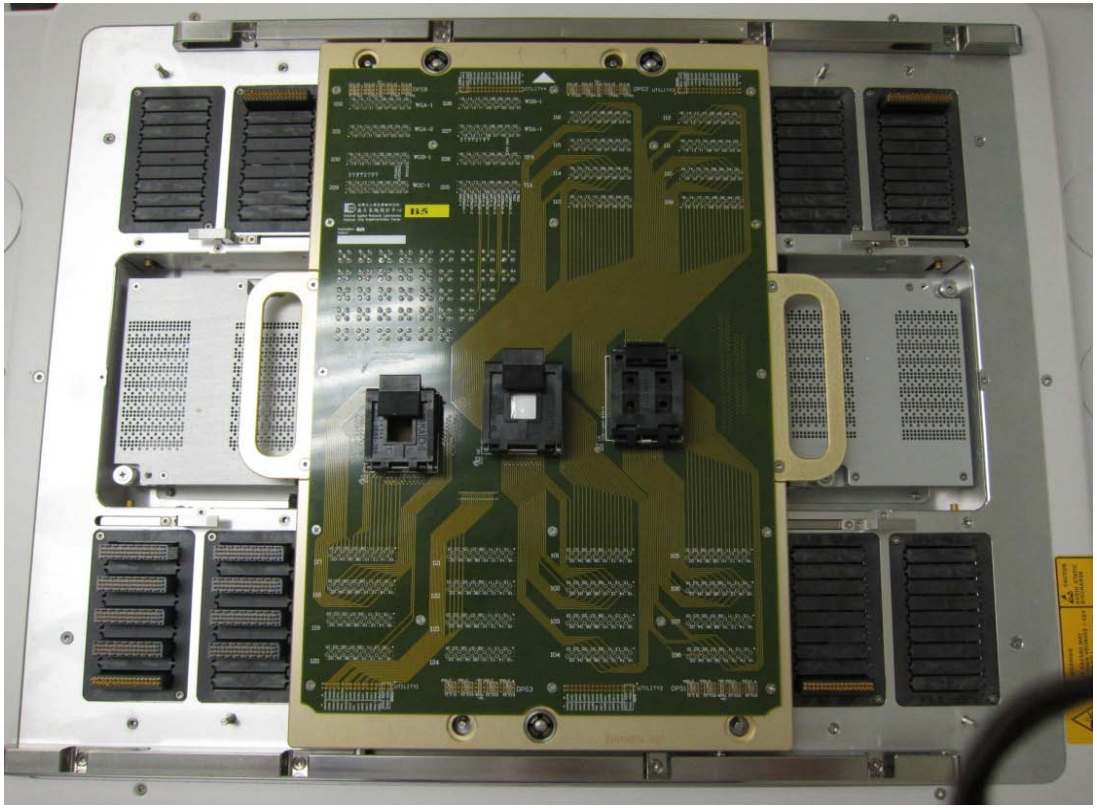
Taped-out via CIC

- Before Taped-out, make sure that
  - Your design is DRC clean.
  - Your design passes the block-box LVS check.
  - Your design meet the timing/power specification.
- When taped-out via CIC, prepare the following:
  - GDSII layout of your design
  - Calibre DRC report file
  - Calibre LVS report file
  - Post-layout timing/power verification result
  - Specification files of used memories

下線準備資料

- 下線所需要上傳的資料有下列五種:
  - 1. 下線報告(Word)
  - 2. layout完成的gds檔
  - 3. DRC.rep(看DRC錯誤的檔案)
  - 4. lvs.rep(有笑臉的檔案)
  - 5. tapeout報告(Word, 附件二)
- 需準備的檔案有下列兩種:
  - 1. 檔名:上傳號碼；內容:學校信箱
  - 2. ok檔；內容:ok
- 上傳方式請參考附件三。

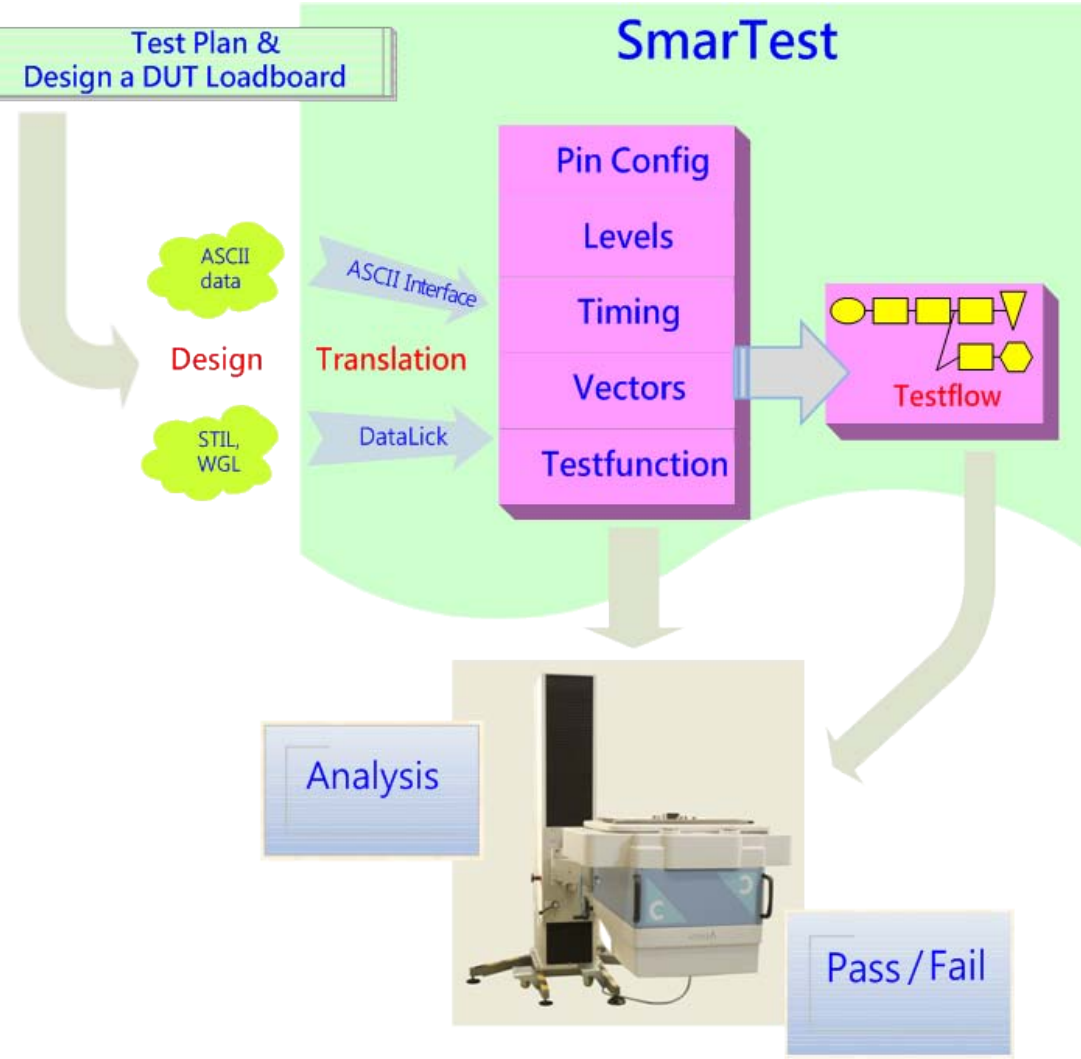
Automatic Test System

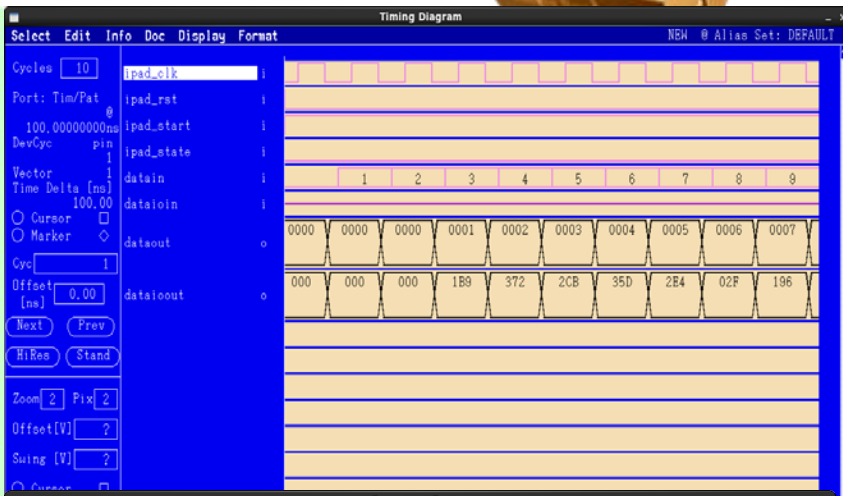


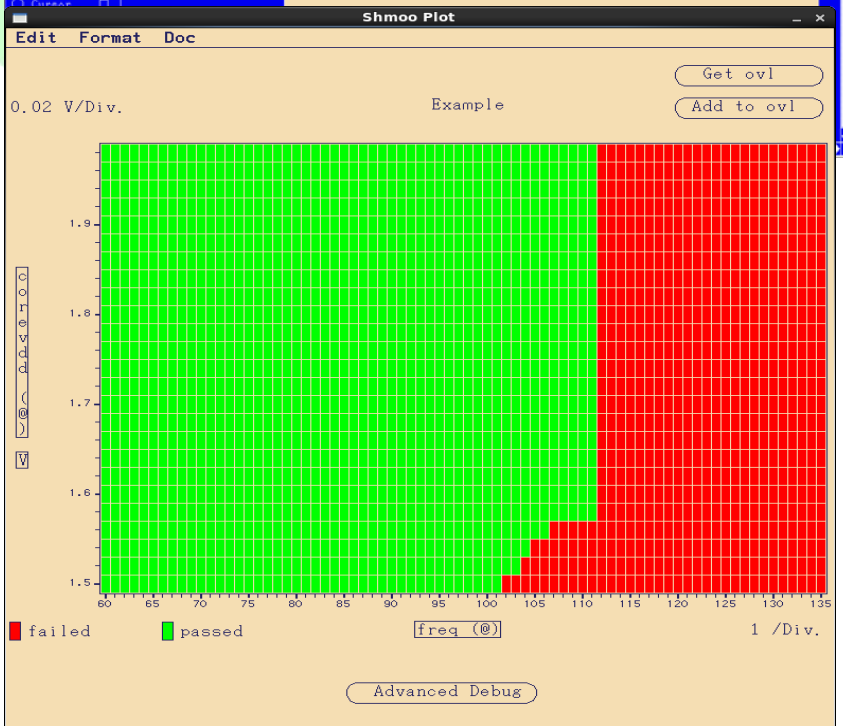
ADVANTEST V93000 PS1600
CIC Package：CQFP, LCC, SB

Ref：NAR Labs 國家晶片系統設計中心

Automatic Test System (Cont.)



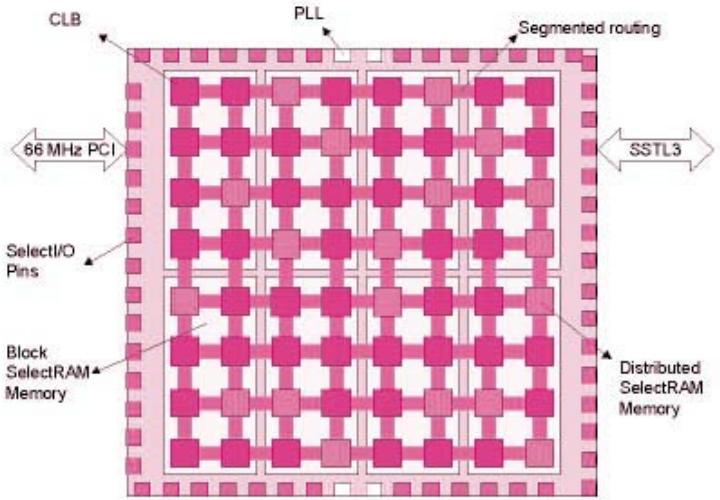




Ref：NAR Labs 國家晶片系統設計中心

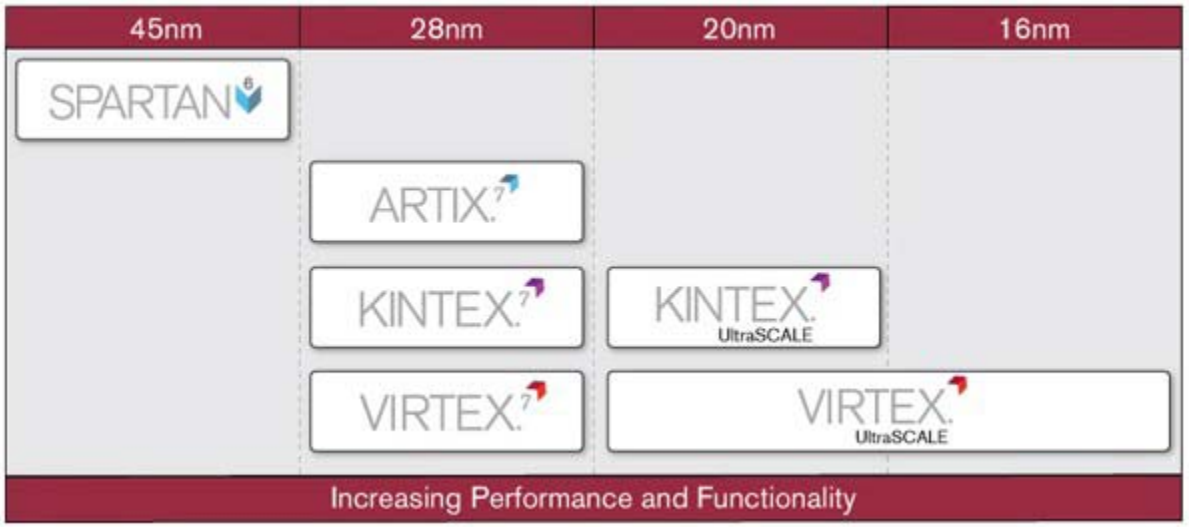
Programmable Logic

- PLD (Programmable Logic Device) according to their structure and density can be divided into three categories
  - SPLD（Simple Programmable Logic Device)
  - CPLD（Complex Programmable Logic Device)
  - FPGA (Field Programmable Gate Array)
- Xilinx
- Altera
- Actel (Microsemi)



Xilinx

	Spartan-6	Artix-7	Kintex-7	Virtex-7
Logic Cells	150,000	215,000	480,000	2,000,000
BlockRAM	4.8Mb	13Mb	34Mb	68Mb
DSP Slices	180	740	1,920	3,600
DSP Performance (symmetric FIR)	140GMACs	930GMACs	2,845GMACs	5,335GMACs
Transceiver Count	8	16	32	96
Transceiver Speed	3.2Gb/s	6.6Gb/s	12.5Gb/s	28.05Gb/s
Total Transceiver Bandwidth (full duplex)	50Gb/s	211Gb/s	800Gb/s	2,784Gb/s
Memory Interface (DDR3)	800Mb/s	1,066Mb/s	1,866Mb/s	1,866Mb/s
PCI Express® Interface	x1 Gen1	x4 Gen2	x8 Gen2	x8 Gen3
Analog Mixed Signal (AMS)/XADC		Yes	Yes	Yes
Configuration AES	Yes	Yes	Yes	Yes
I/O Pins	576	500	500	1,200



Ref：http://www.xilinx.com/products/silicon-devices/fpga/index.htm

Xilinx ISE

Create an HDL Source

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    09:58:18 12/11/2007
// Design Name:
// Module Name:    counter
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module counter(
    input CLOCK,
    input DIRECTION,
    output [3:0] COUNT_OUT
    );
endmodule
```

Implement Design and Verify Constraints

tutorial Project Status (12/11/2007 - 11:35:57)			
Project File:	tutorial.ise	Current State:	Placed and Routed
Module Name:	counter	• Errors:	No Errors
Target Device:	xc3s200-4ft256	• Warnings:	No Warnings
Product Version:	ISE 10.1 - Foundation Simulator	• Routing Results:	All Signals Completely Routed
Design Goal:	Balanced	• Timing Constraints:	All Constraints Met
Design Strategy:	Xilinx Default (unlocked)	• Final Timing Score:	0 (Timing Report)

tutorial Partition Summary
No partition information was found.

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	4	3,840	1%	
Number of 4 input LUTs	4	3,840	1%	
Logic Distribution				

Xilinx ISE (Cont.)

Assigning Pin Location Constraints

Download Design to the Demo Board

Altera

High-End FPGAs

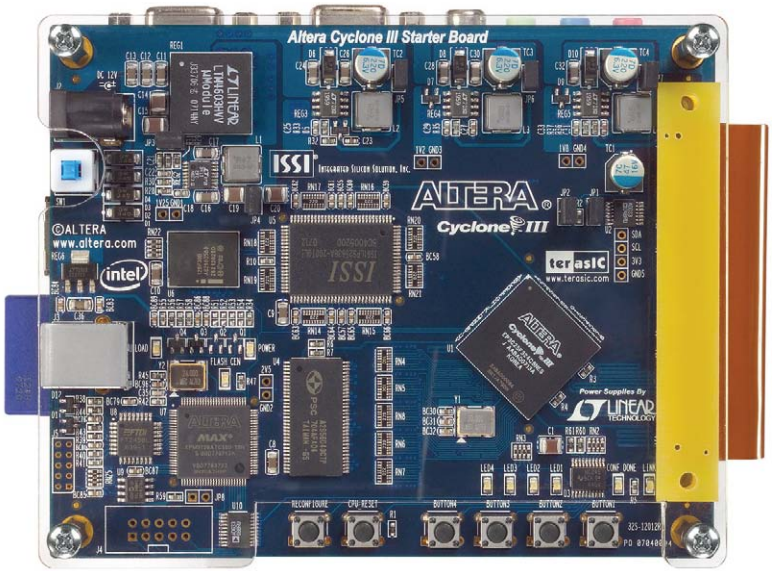
- Highest bandwidth, highest density FPGAs
- Integrated transceiver variants
- Design entire systems on a chip

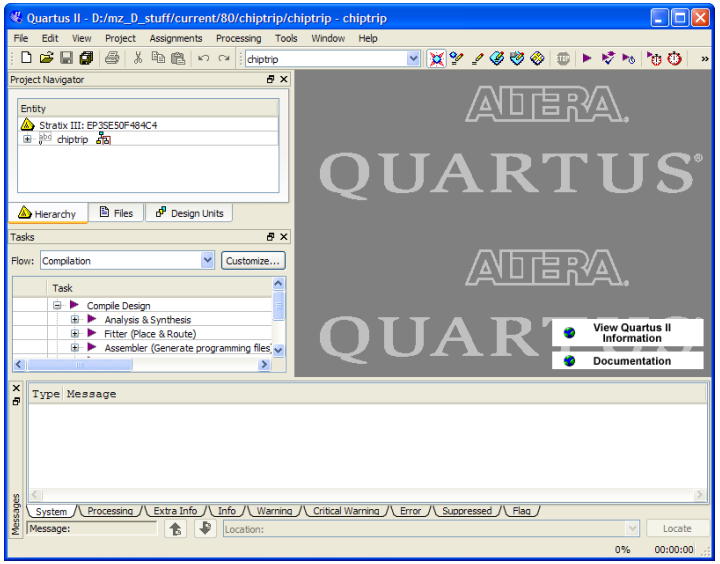
Midrange FPGAs

- Balanced cost, power, and performance FPGAs
- Integrated transceiver and processor variants
- Comprehensive design protection

Lowest Cost and Power FPGAs

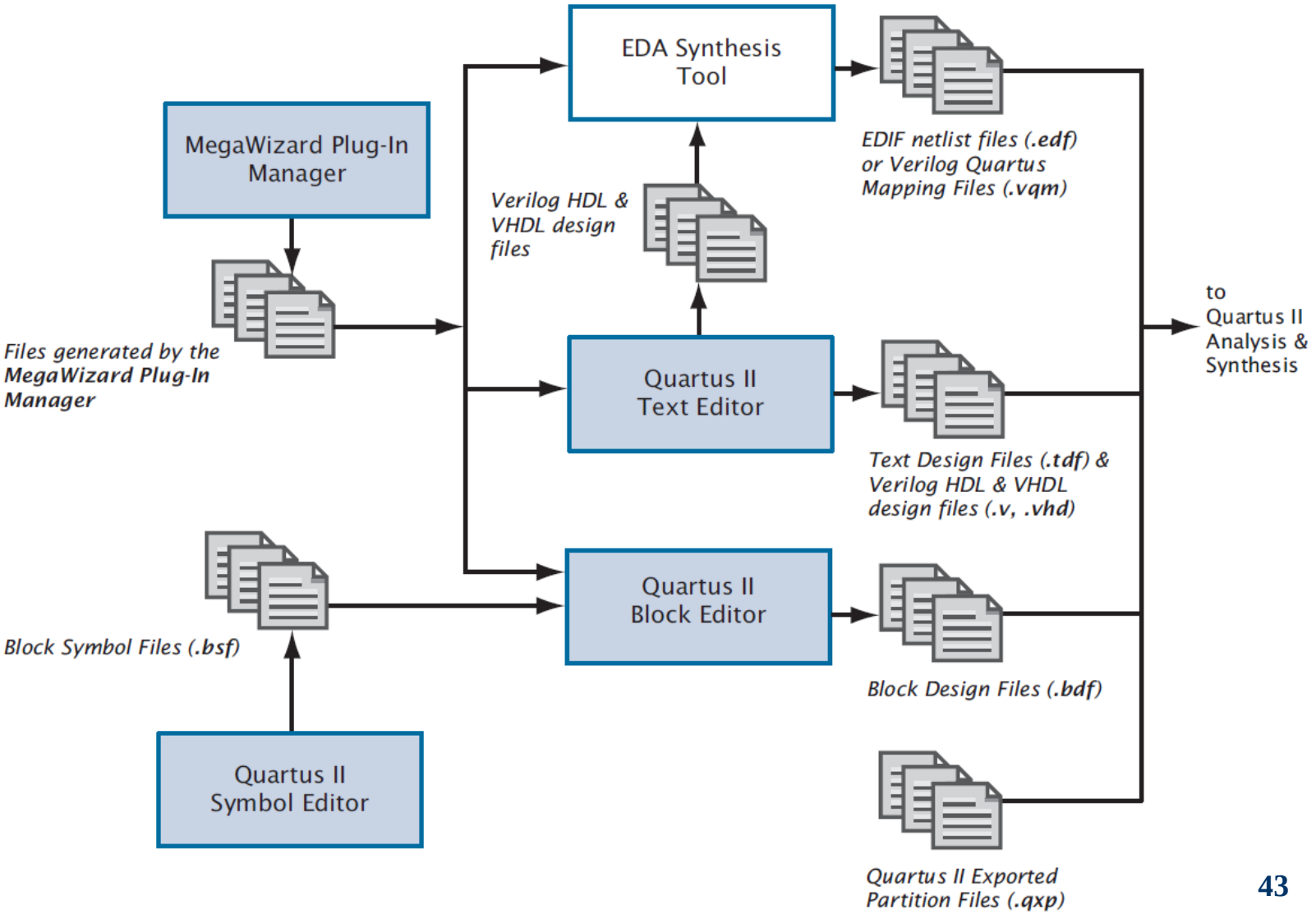
- Lowest system cost and power FPGAs
- Integrated transceiver and processor variants
- Fastest time to market





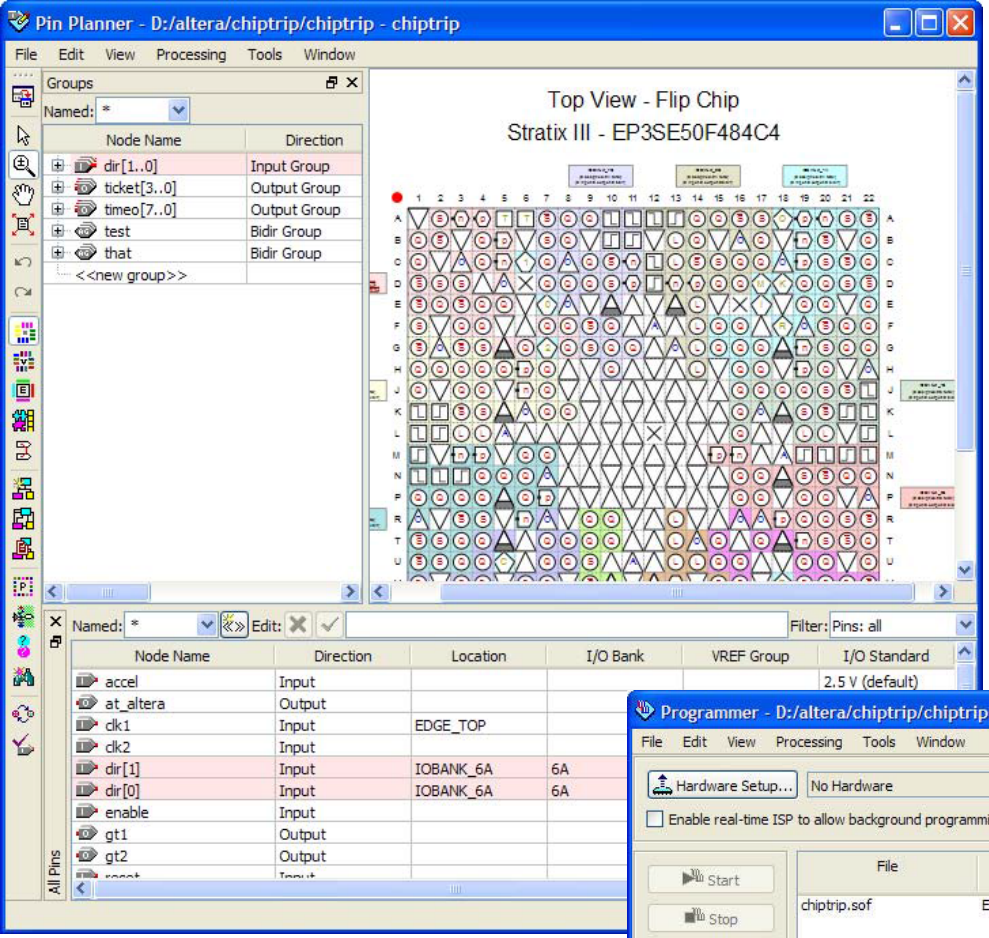
Ref：http://www.xilinx.com/products/silicon-devices/fpga/index.htm

QUARTUS II Design Entry Flow

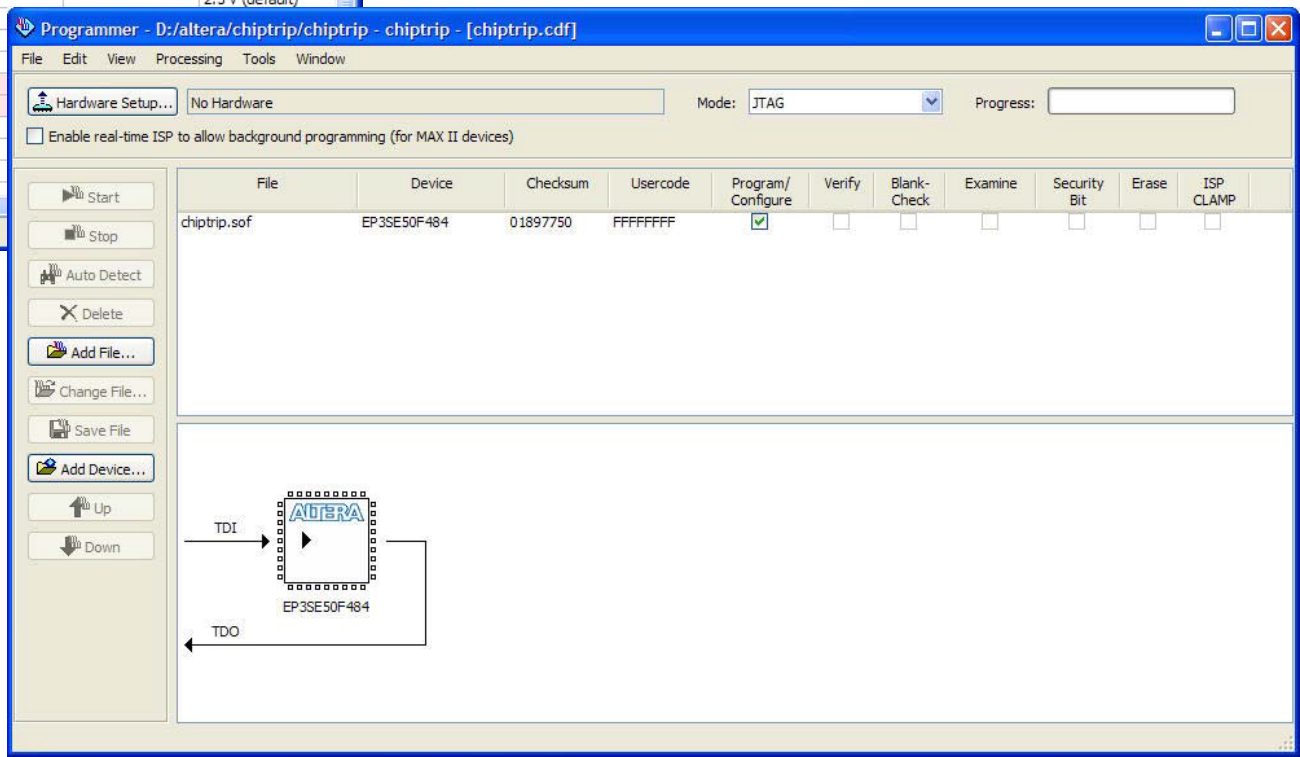


QUARTUS II

Pin Planner

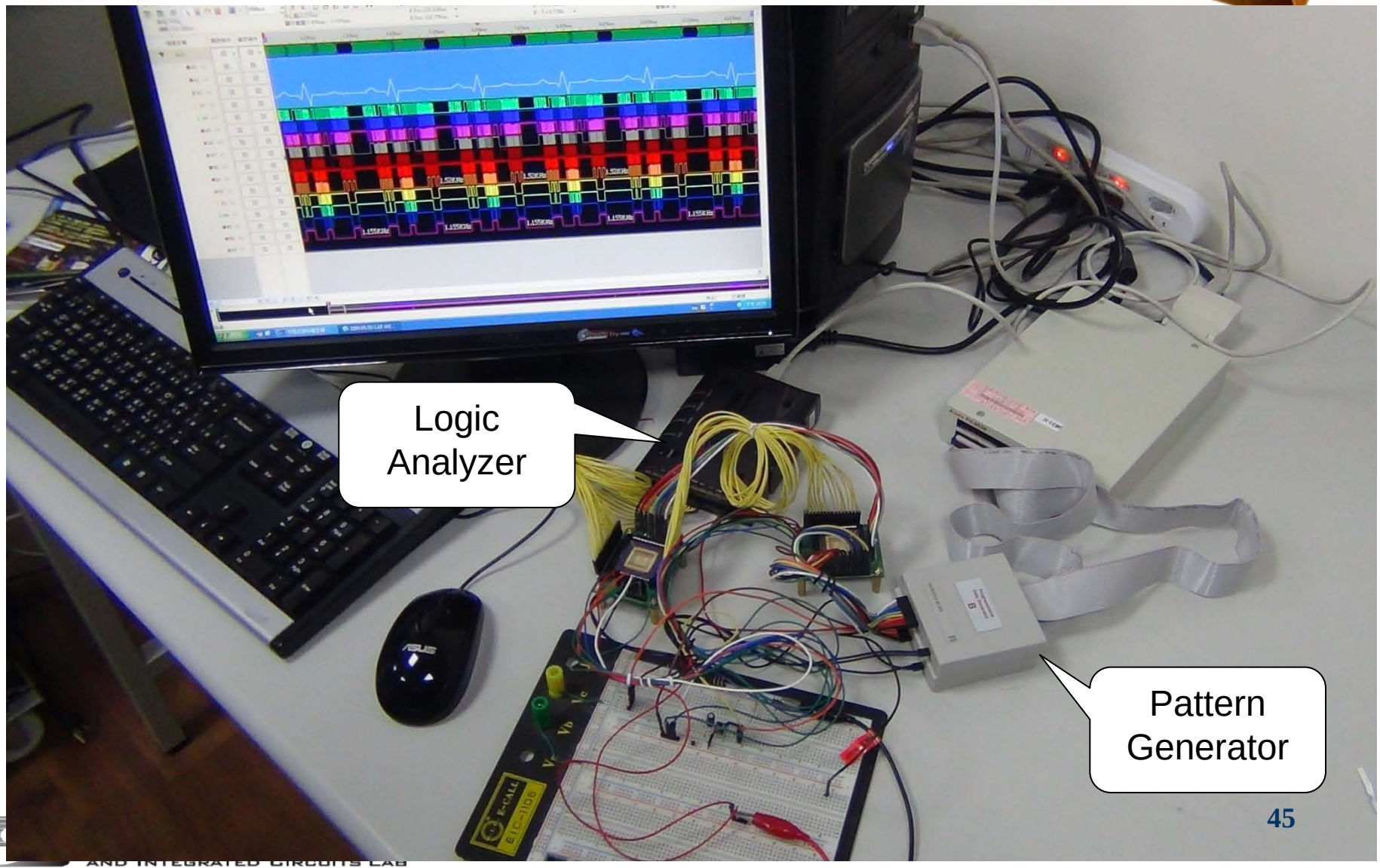


Programmer

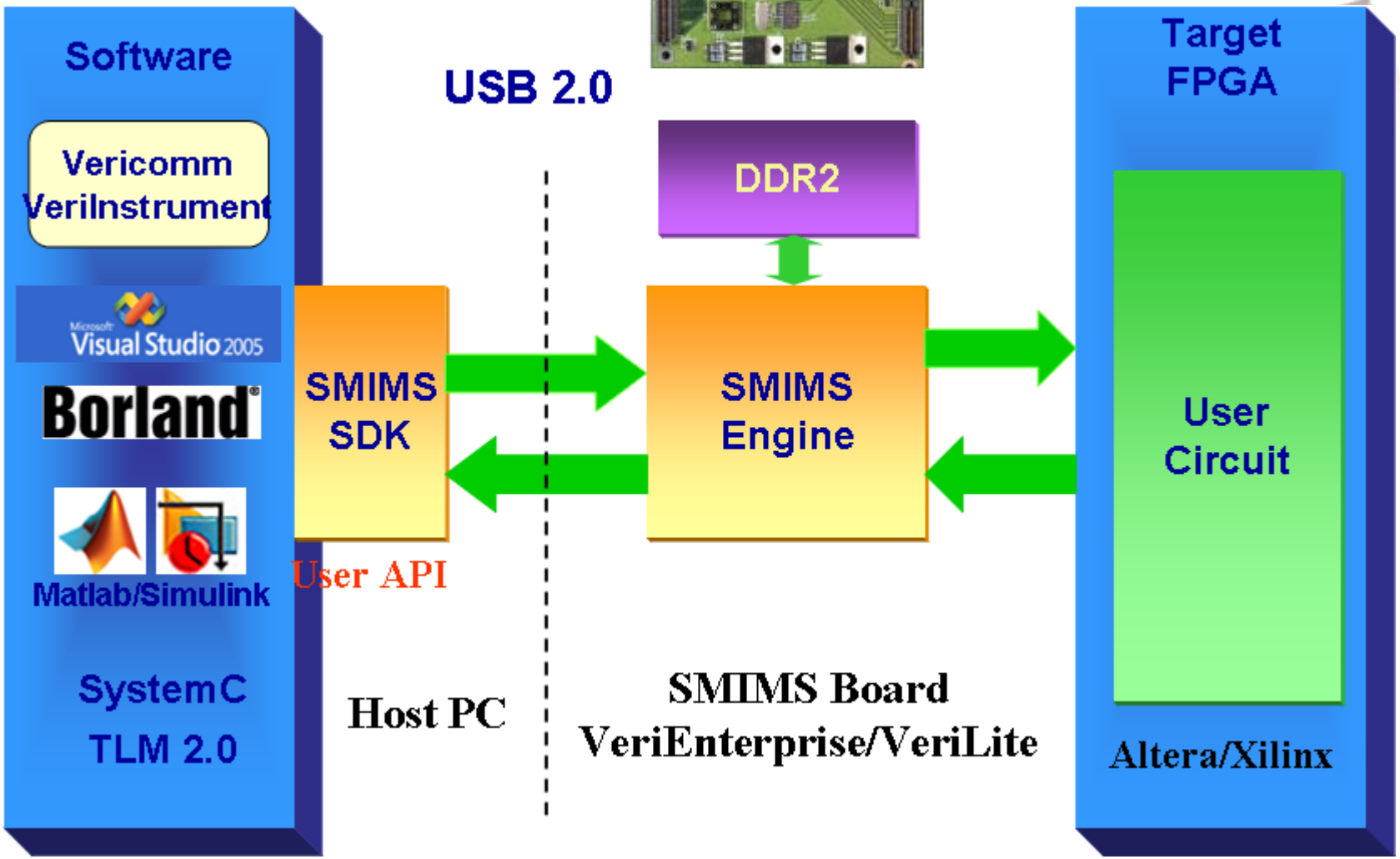


QUARTUS II

Measurement



SMIMS



Ref：北瀚科技 http://tw.smims.com/

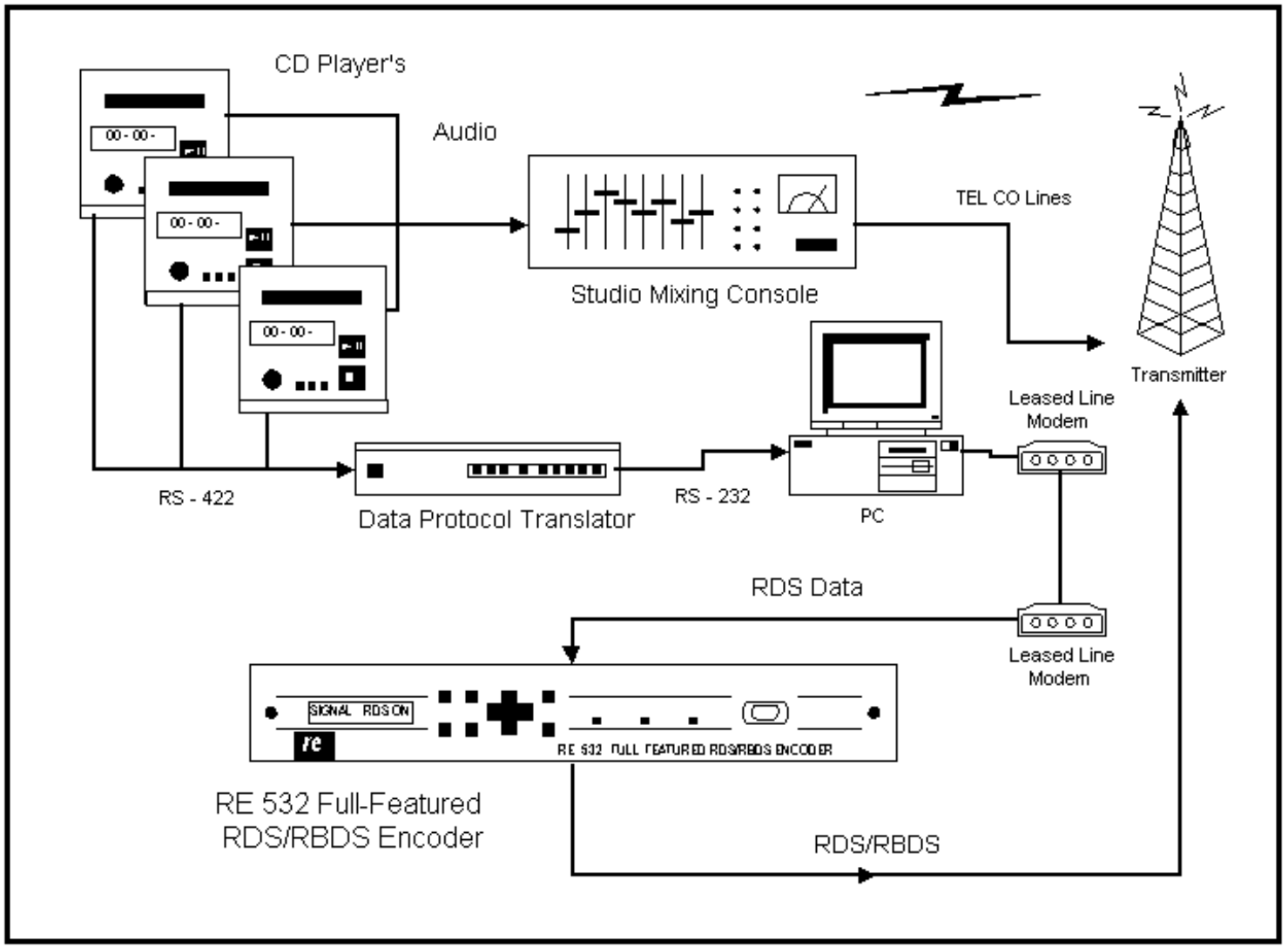
Outline

1. Integrated Circuit
2. Chip Design
3. Application

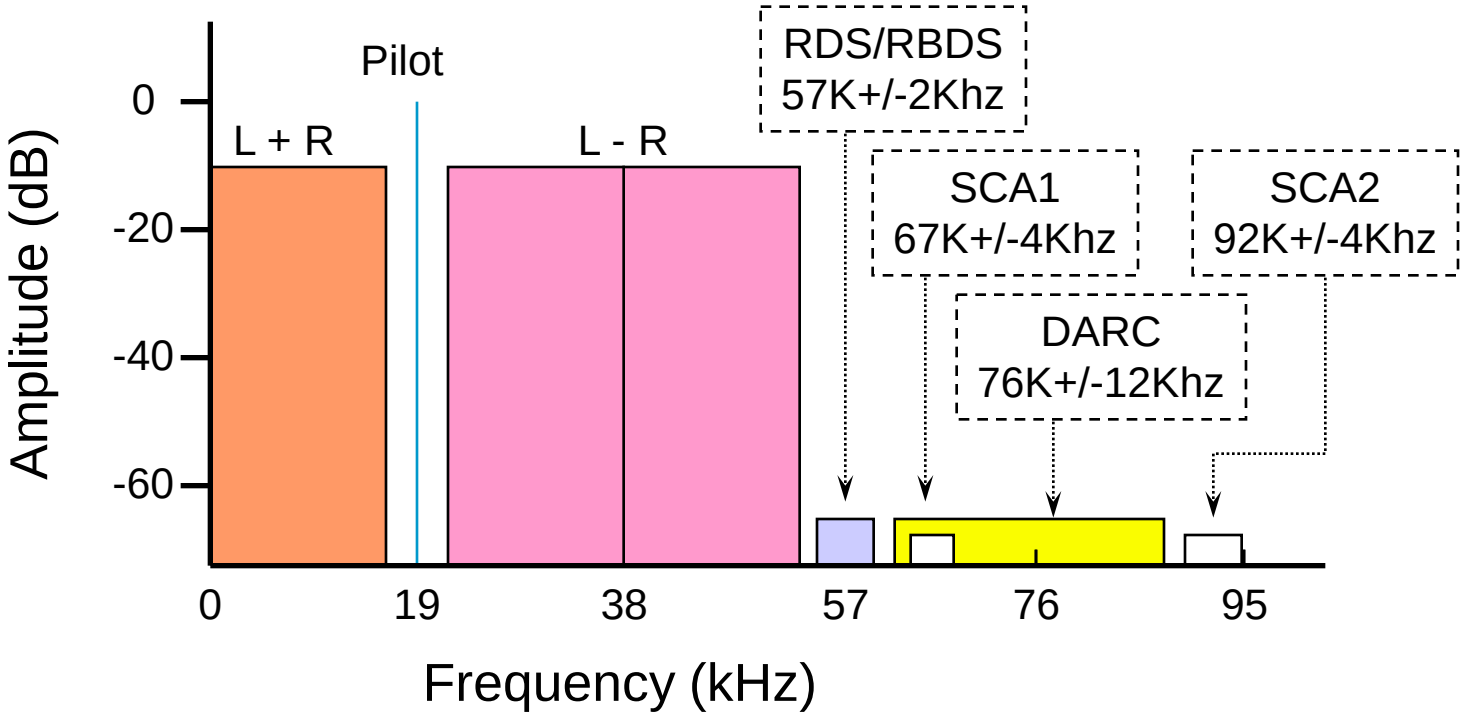
System Application

- Radio Data System
- 智慧電子國家型科技計畫(NPIE) -- Interactive Intelligent Healthcare System
- PCB board Circuits Design
- IC Samples

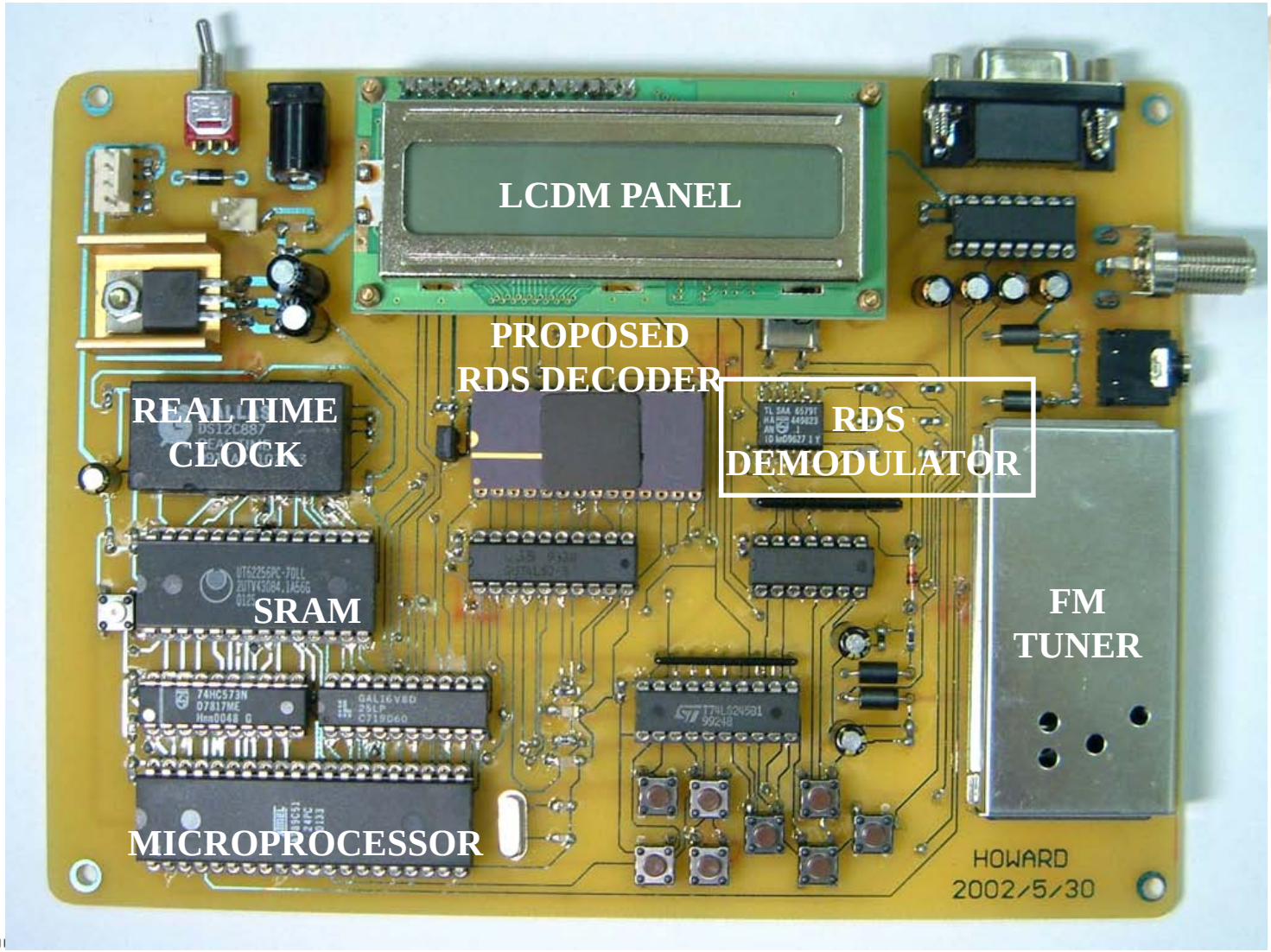
Digital RDS Demodulation in FM Subcarrier Systems



Radio Data System



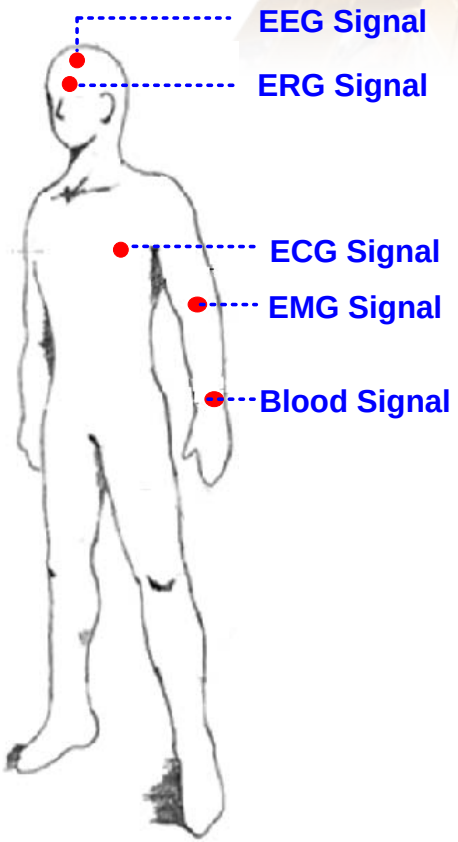
RDS Receiver Physical Circuit



Measurement Environment

Healthcare Monitoring

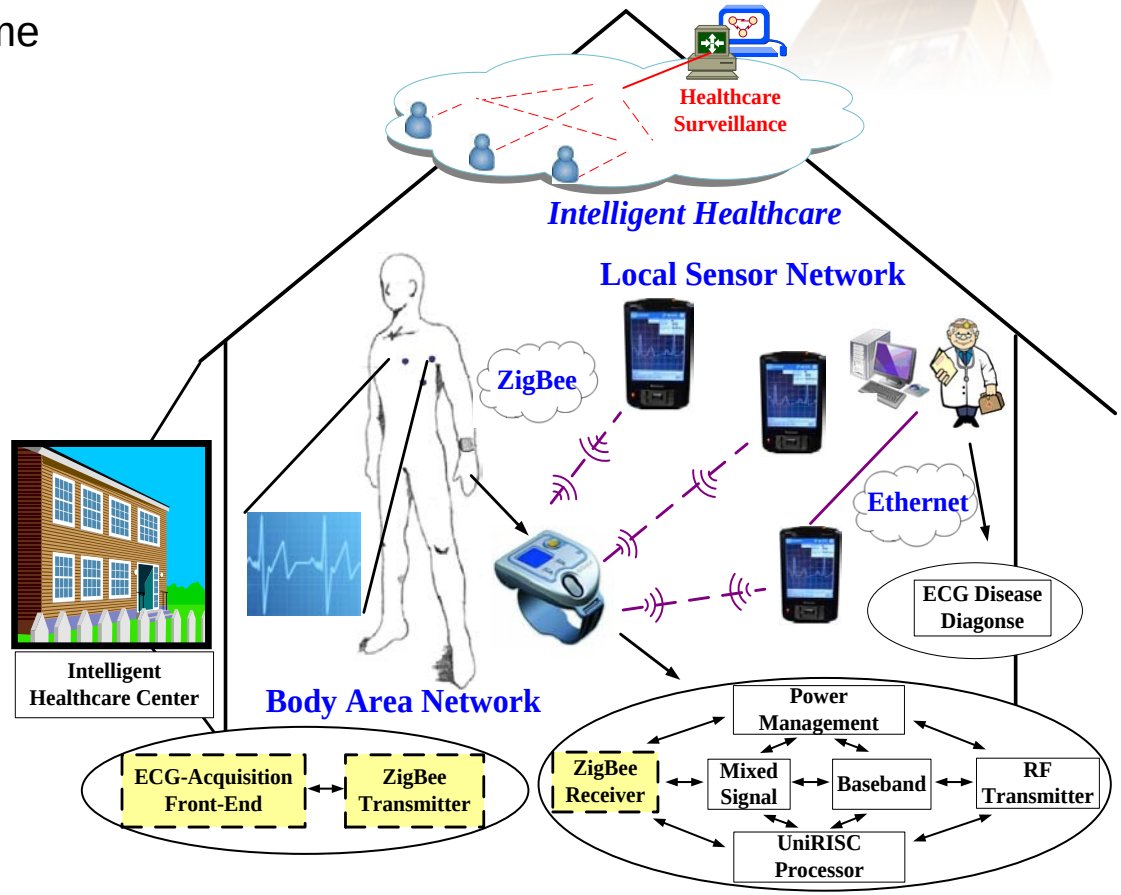
- Motivation
  - Aging Population, Intensity lifestyle
    - Pressure, Nervousness, Disturbance
    - Chronic Cardiovascular Diseases
  - Bio-microsystem application
    - EEG, ERG, ECG, EMG, Blood.
- Intelligent Healthcare Monitoring
  - Interactive, Low Power, Wireless SoC
    - IEEE 802.15.4 ZigBee Application
    - 2.4GHz ISM Band



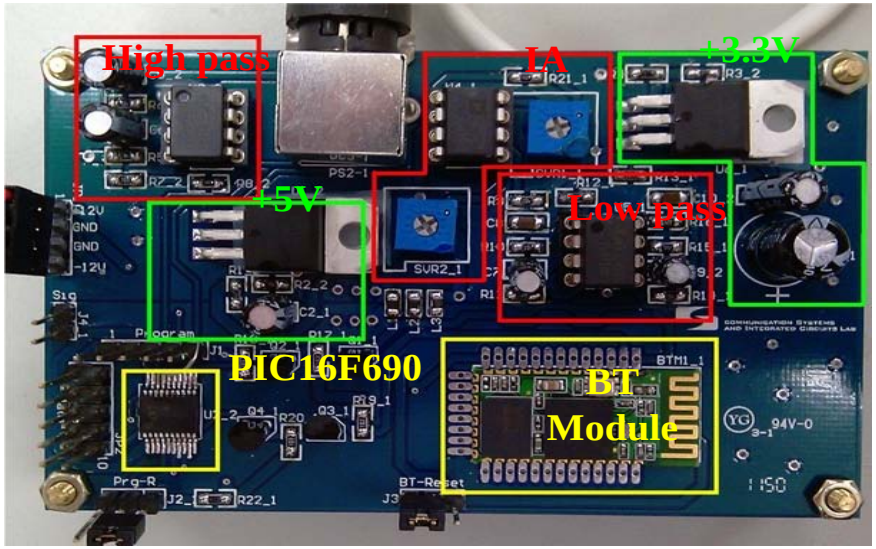
Ref：國立成功大學，李順裕教授，NPIE生醫電子計畫

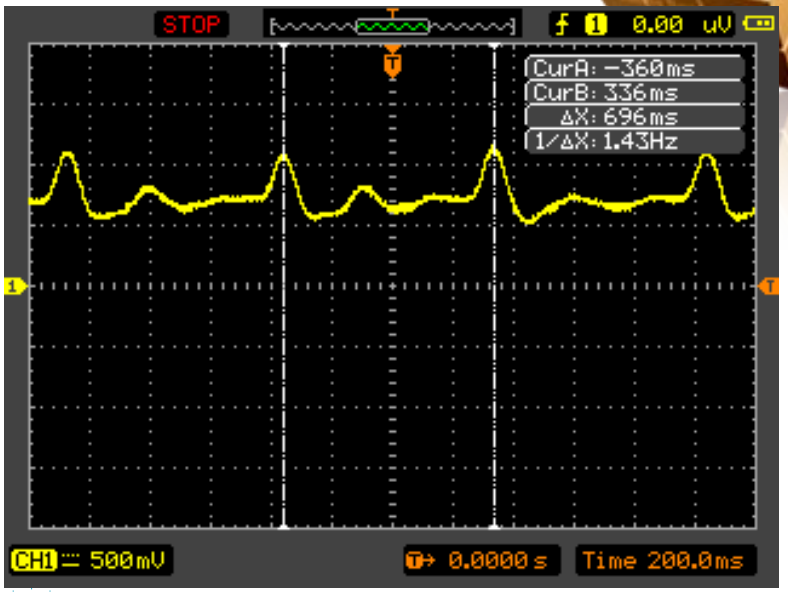
Interactive Intelligent Healthcare System

- Targets
  - Low Power, Anywhere, Anytime
  - Long-term Monitoring
- Body Area Network
  - Near-Body Application
  - Acquisition Node
    - – Wearable Device (watch)
- Local Sensor Network
  - Intermediate Interface
  - Wearable Device
    - – Portable Facility (PDA)

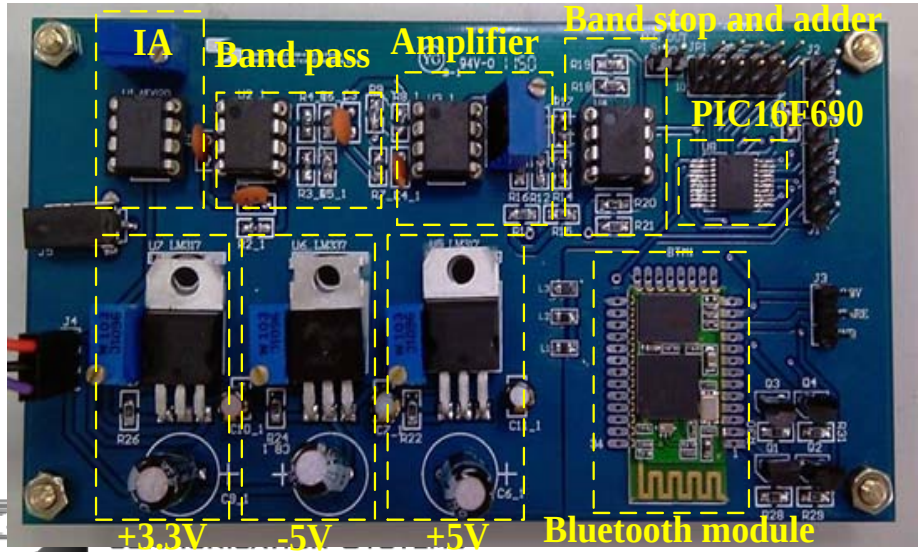


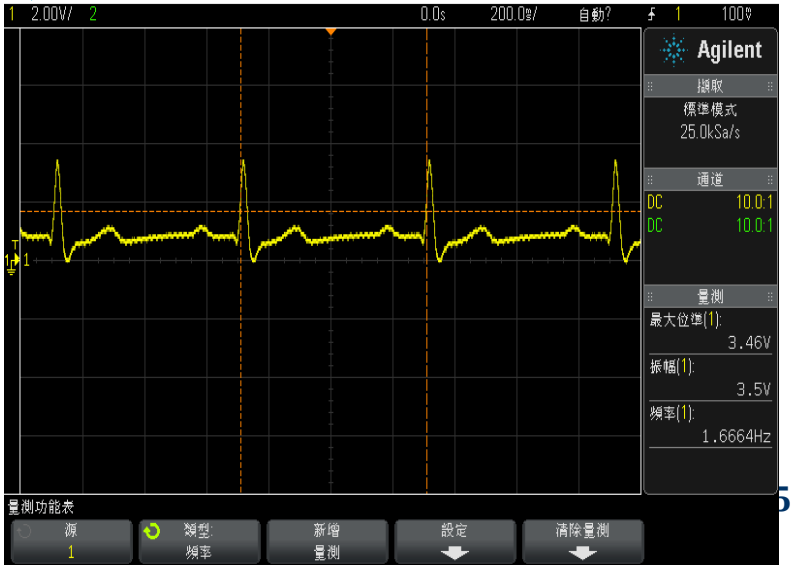
SpO_2 & ECG Circuits Design





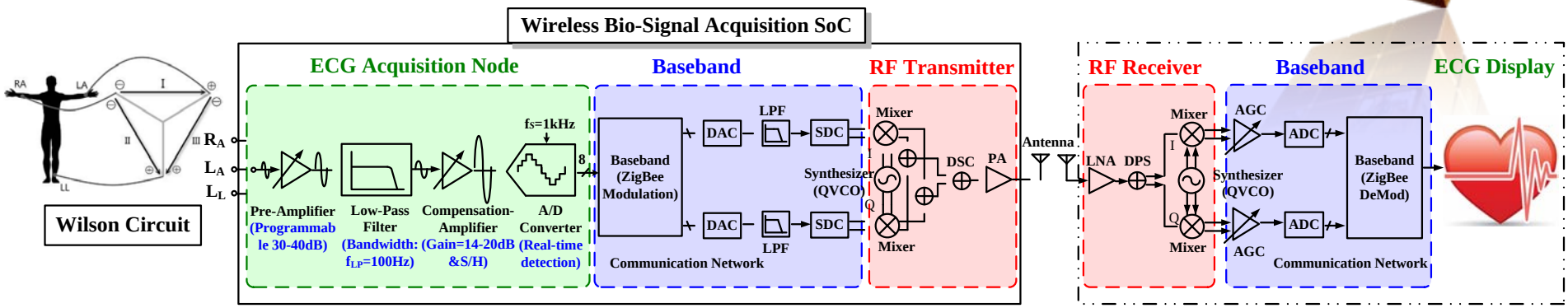
SpO_2



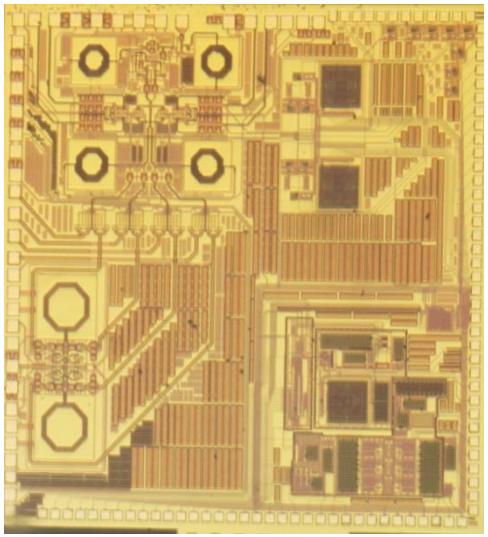


ECG

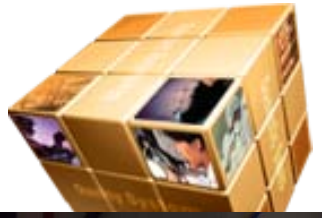
System Block Diagram

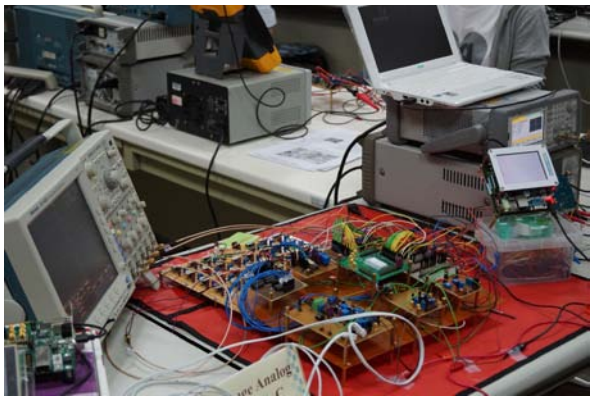


- Transmitter : Wireless Bio-Signal Acquisition SoC (WBSA-SoC)
  - AFE : PreAmp., Filter, PostAmp., 8-bit SAADC
  - Baseband : ZigBee Spread Spectrum Technology
  - RF Front-end : VCO, Up-Mixer, PA
- Receiver: ARM Display
  - RF Front-end : LNA, Down-Mixer
  - Mixed-Mode Board: BPF, AGC, ADC
  - Based-Band & Display : ZigBee Demod. & ARM-base Display

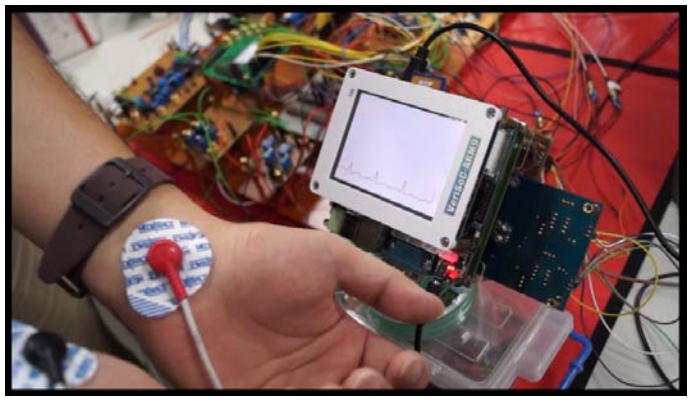


System Experiment Result



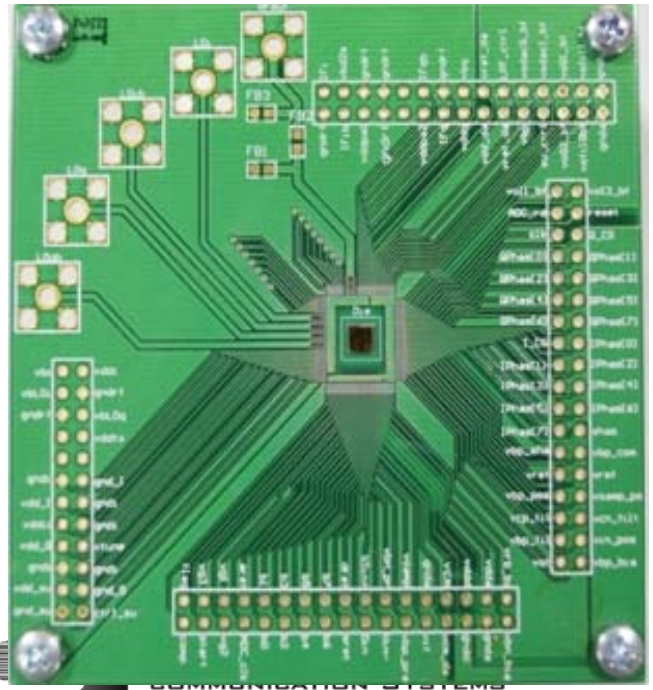


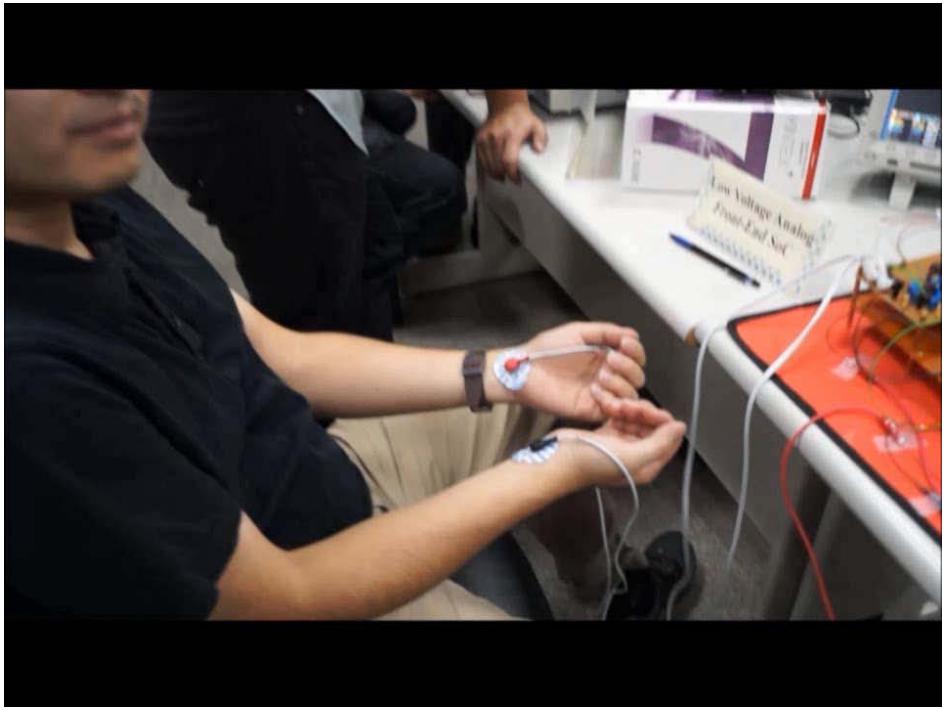
Verification Setup



Measurement Setup

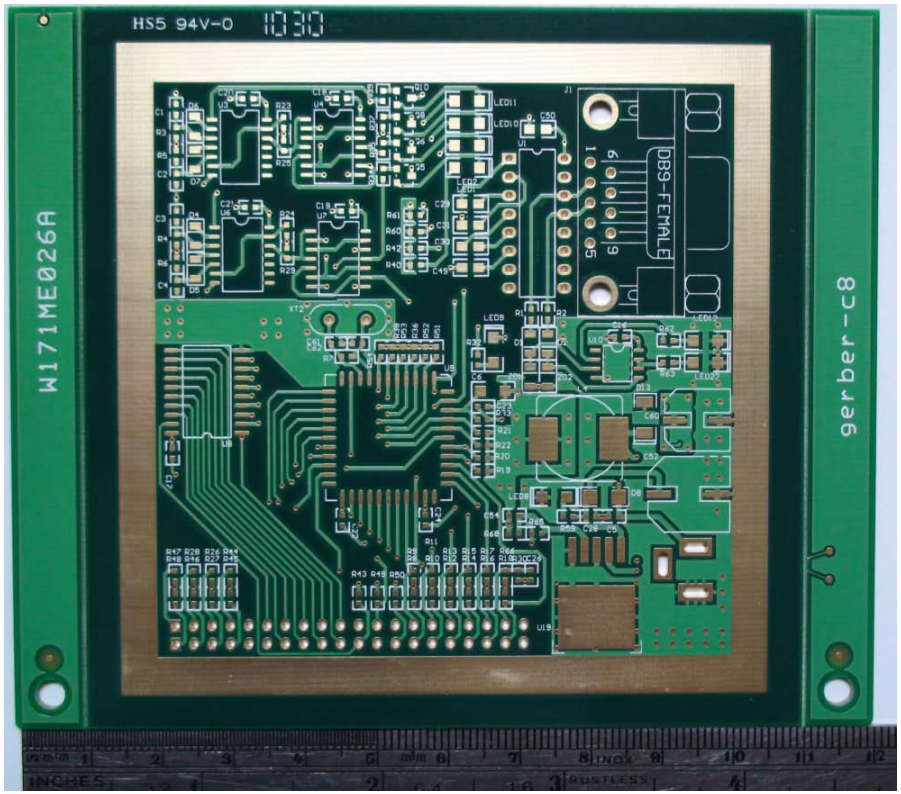
Display with ARM Platform

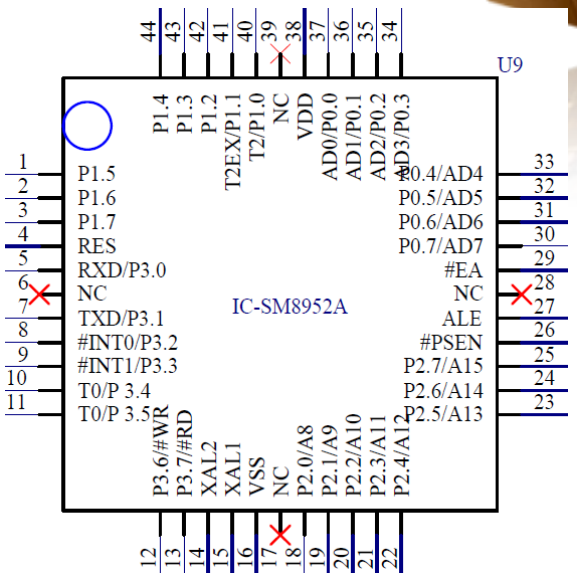


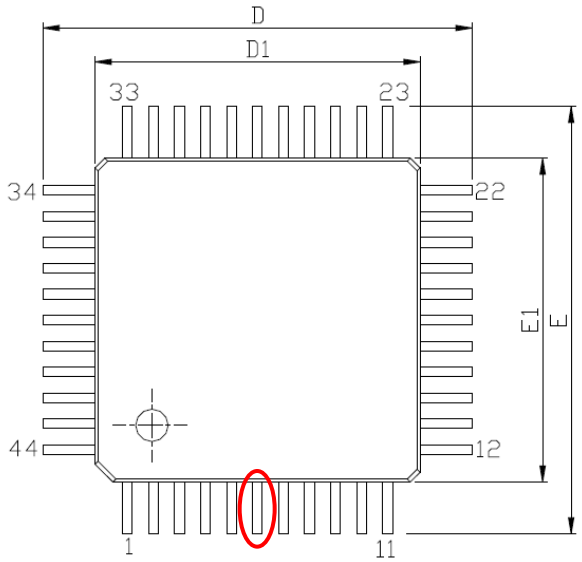


Video

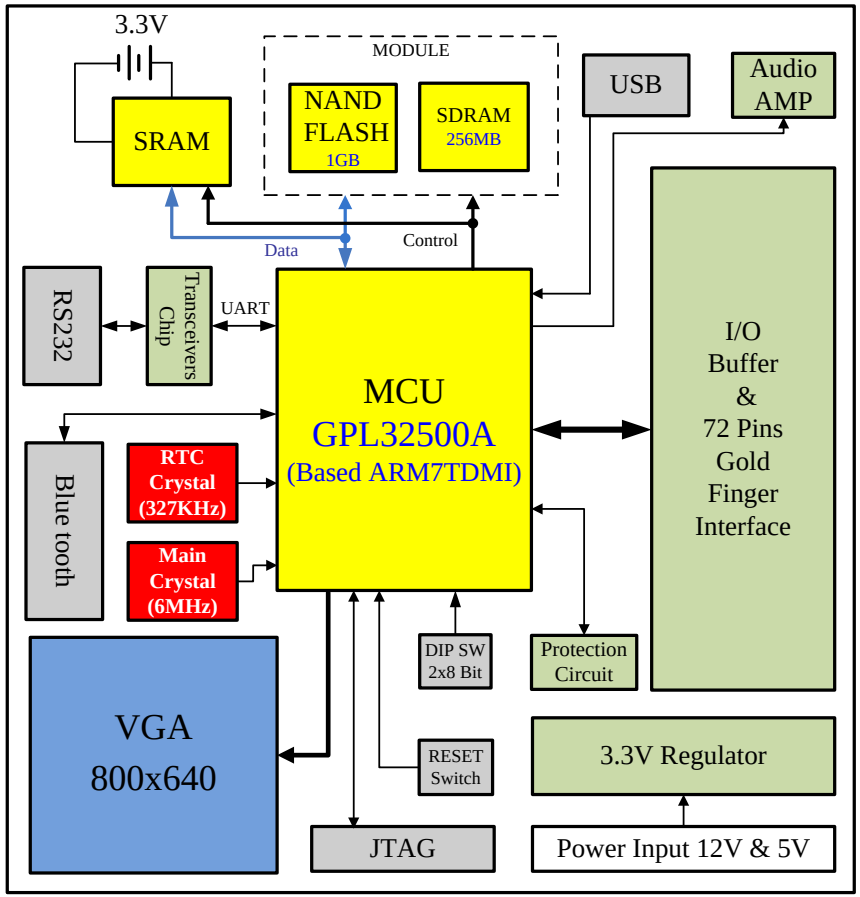
經濟部標準檢驗局電磁相容(EMC)設計競賽

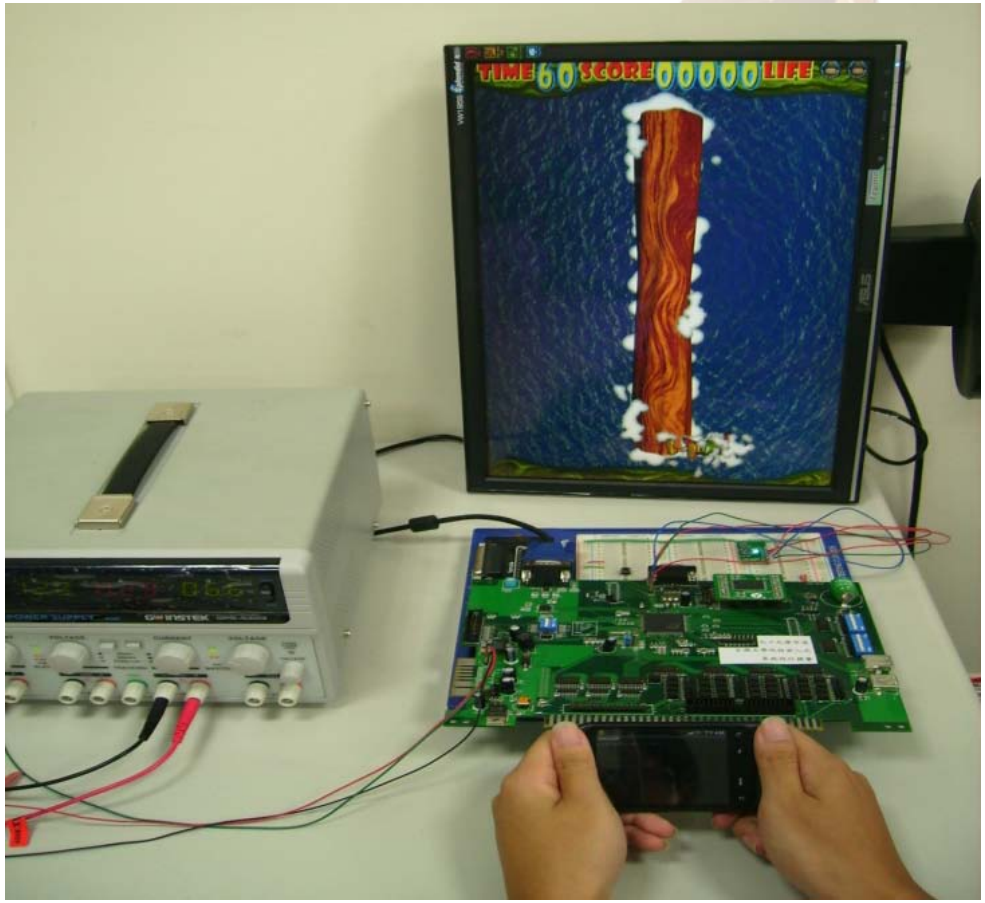






Embedded Development Platform





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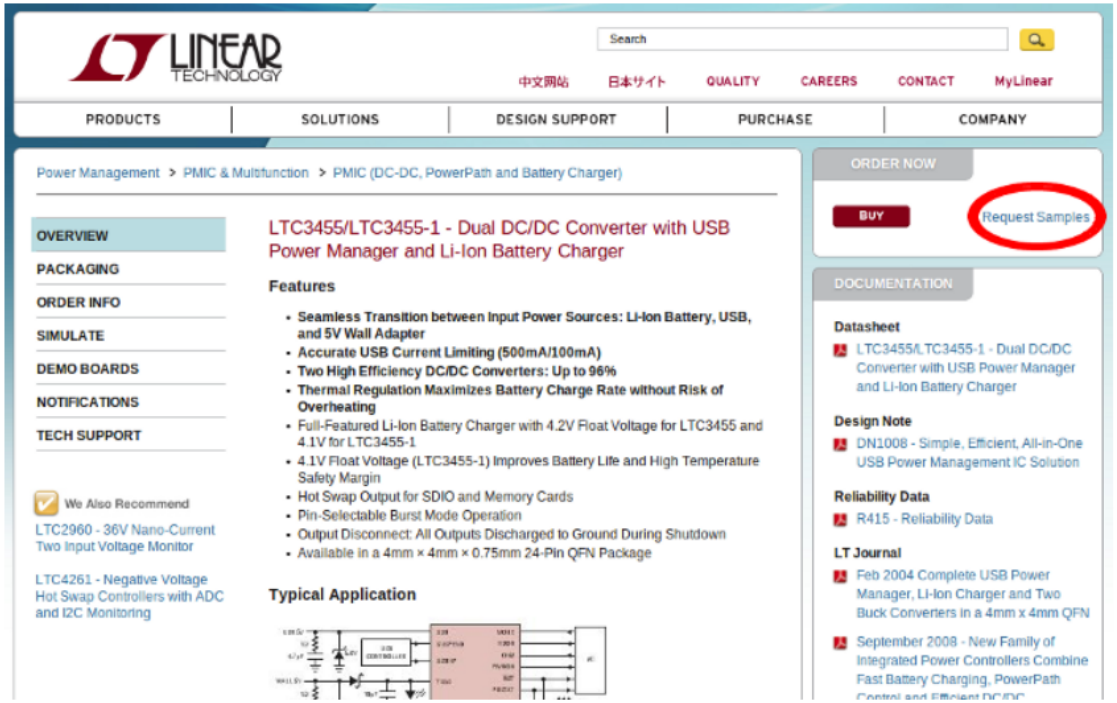
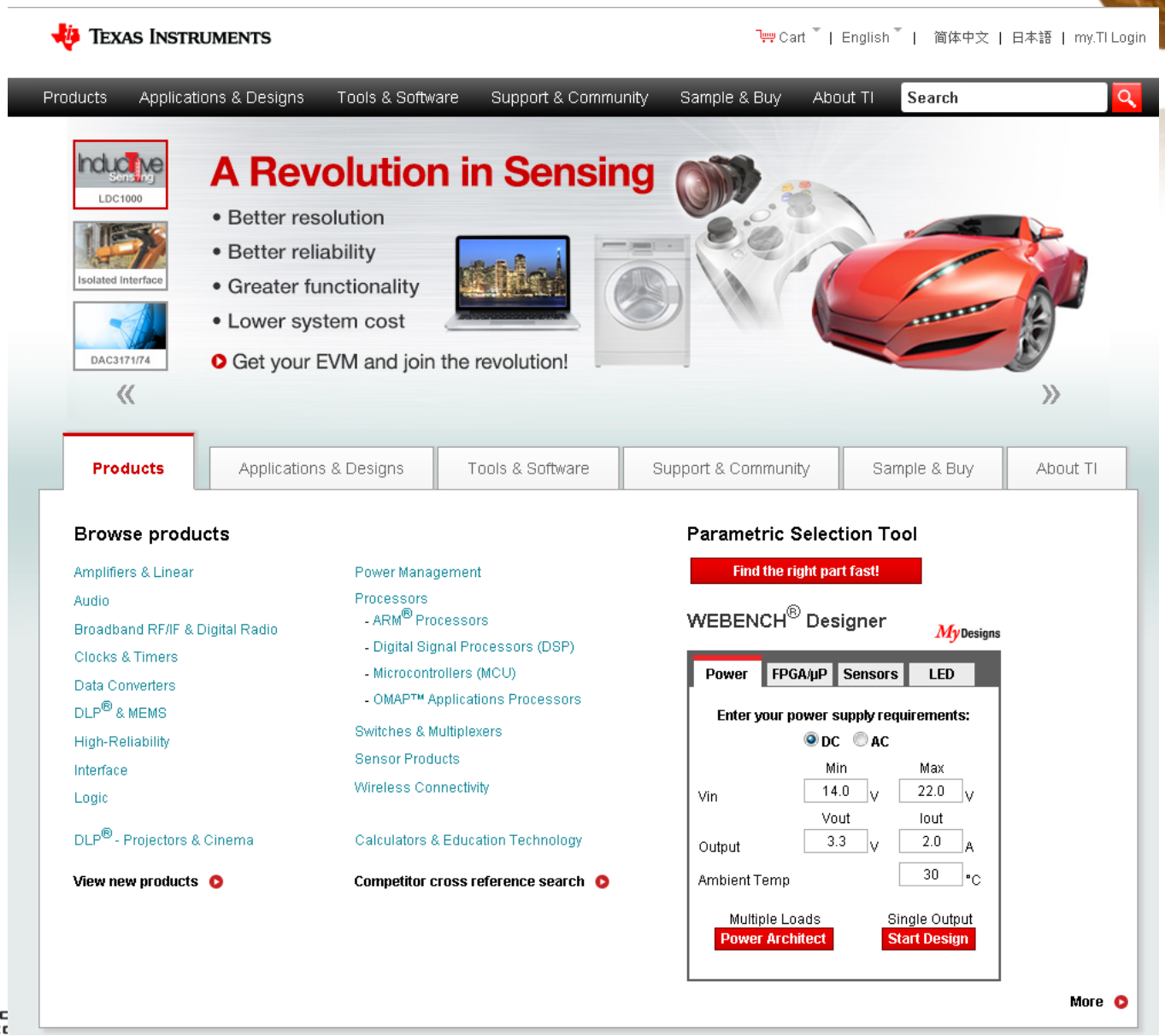


Analog Device

Texas Instruments



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